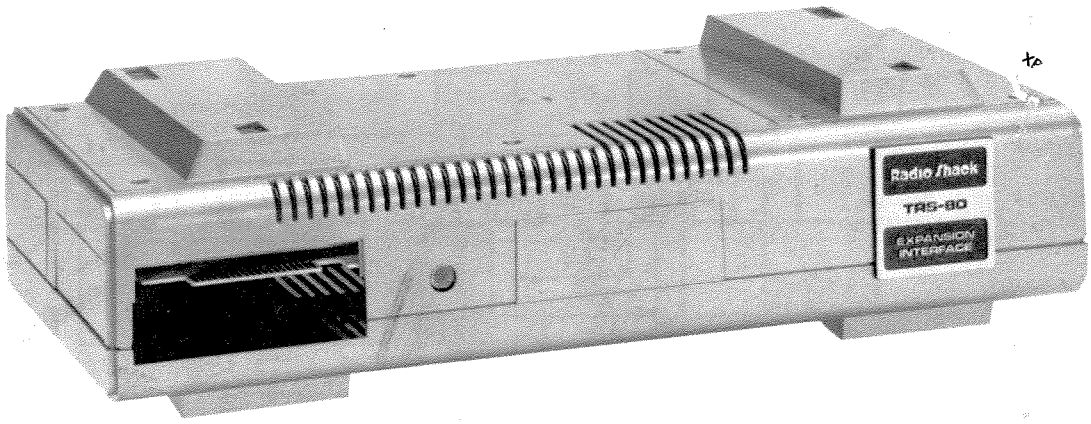
Radio Shack®

Service Manual

26-1140

EXPANSION INTERFACE

Catalog Number 26-1140



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INTRODUCTION

Before you service the TRS-80 Expansion Interface, you should read and understand both of the TRS-80 Technical Manuals and the Quality Assurance Test Program Service Manual. These Manuals provide detailed service and trouble-shooting information for the TRS-80 Microcomputer which generates all of the signals to the Expansion Interface. In a TRS-80 System environment, the Quality Assurance Test Program automatically checks the Expansion Interface Address Decoder and the memory associated with it.

The Expansion Interface can support ØK, 16K or 32K of dynamic RAM. The two RAM select lines are 32K and 48K. You can find the details of their generation in the Address Decoder section of this Manual.

This Manual also provides a Block Diagram (as shown in Figure 1); functional descriptions of the different circuits and a Parts List. An exploded view of the Expansion Unit; top and bottom views of the P. C. Board and a Schematic Diagram of the TRS-80 Expansion Interface are also provided. An Appendix is included that contains a reprint of the Western Digital Data Sheet for the Floppy Disk Formatter/ Controller (FD1771 A/B - 01).

To aid in servicing the TRS-80 Expansion Interface, you'll also need the Shugart Associates OEM and Service Manuals for the SA400 minifloppy™ Diskette Storage Drive.

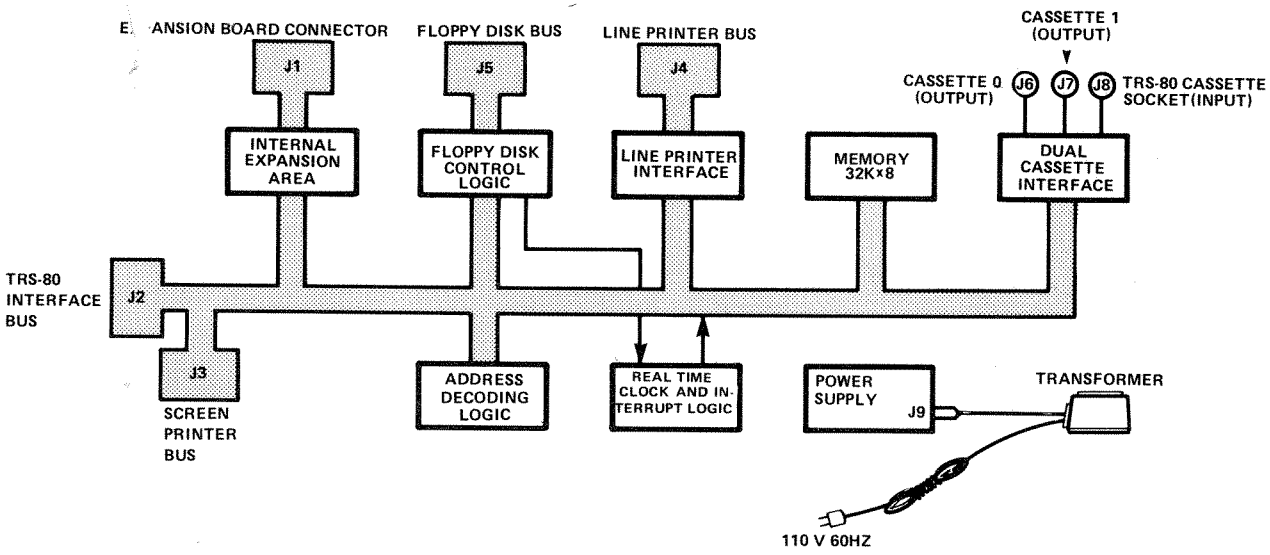


FIGURE 1. BLOCK DIAGRAM OF EXPANSION INTERFACE

ADDRESS DECODER

NOTE

Refer to the TRS-80 Technical Manual, "Theory, Parts List, Schematics", page 8 and to the Schematic Diagram (Sheet 3) in this Manual.

The Address Decoder logic consists of Z42, Z43, Z32 and one inverter from Z23.

CAUTION

Excessive line noise or power interruptions may cause the RAMs to change states, resulting in unpredictable behavior.

Z43 is a dual 2 line to 4 line demultiplexer. One half of this package is used to select 16K increments of memory space. The input signals to this section are RAS*, A14 and A15. RAS* serves as a valid memory address signal, indicating that the addresses have stabilized when it is logical "Ø". Table 1 summarizes the input/output combinations.

Pins 6 and 7 are used to select the 32K and 48K rows of dynamic RAM respectively. Pin 4 is looped back to the second half of Z43. There, it is combined with the output of NAND gate Z42 to give a logical "Ø" on Pin 12 when A11, A14, A15 and RAS* are logical "Ø" and A5, A6, A7, A8, A9, A10, A12 and A13 are logical "1". Pin 12 is a logical "1" at all other times. Pin 5 is not used. It is shown in Table 1 only to show continuity of the input/output combinations.

The signal from Pin 12 of Z43 is combined with A2, A3, WR* and inverted RD* to produce the signals shown in Table 2.

INPUTS			OUTPUTS				
RAS*	A15	A14	Z43 Pin 4	Z43 Pin 5	Z43 Pin 6	Z43 Pin 7	Address Range Selected
1	X	X	1	1	1	1	None
Ø	Ø	Ø	Ø	1	1	1	ØØØØ-3FFF
Ø	Ø	1	1	Ø	1	1	4ØØØ-7FFF
Ø	1	Ø	1	1	Ø	1	8ØØØ-BFFF
Ø	1	1	1	1	1	Ø	CØØØ-FFFF

Note: In the Table, X = Don't care.

TABLE 1

INPUT					OUTPUT									
Z43 PIN 12	RD*	WR*	A3	A2	Z32 PIN 7	Z32 PIN 6	Z32 PIN 5	Z32 PIN 4	Z32 PIN 9	Z32 PIN 10	Z32 PIN 11	Z32 PIN 12	SIGNAL GENERATED	SIGNAL TO
1	X	X	X	X	1	1	1	1	1	1	1	1	NONE	——
Ø	Ø	1	Ø	Ø	Ø	1	1	1	1	1	1	1	37EØ READ	INTERRUPT LOGIC
Ø	Ø	1	Ø	1	1	Ø	1	1	1	1	1	1	37E4 READ	——
Ø	Ø	1	1	Ø	1	1	Ø	1	1	1	1	1	37E8 READ	PRINTER LOGIC
Ø	Ø	1	1	1	1	1	1	Ø	1	1	1	1	37EC READ	FLOPPY DISK CONTROLLER
Ø	1	Ø	Ø	Ø	1	1	1	1	Ø	1	1	1	37EØ WRITE	DRIVE SELECT
Ø	1	Ø	Ø	1	1	1	1	1	1	Ø	1	1	CSW	CASSETTE RELAY
Ø	1	Ø	1	Ø	1	1	1	1	1	1	Ø	1	37E8 WRITE	PRINTER LOGIC
Ø	1	Ø	1	1	1	1	1	1	1	1	1	Ø	37EC WRITE	FLOPPY DISK CONTROLLER

NOTE: X = Don't Care

TABLE 2

DUAL CASSETTE PORT

NOTE

Refer to the TRS-80 Technical Manual "Theory, Parts List, Schematics", pages 23 through 26.

The Expansion Interface provides the capability of controlling two cassette recorders. The circuitry required in the Expansion Interface to accomplish this is an input connector (J8), a four pole double throw relay, a relay driver, a D type latch and two output connectors (J6 and J7). This circuitry simply takes the cassette output signals from the TRS-80 and switches them to one of two cassette output jacks, dependent upon the state of the D type latch. The state of this flip-flop is changed by writing to memory address 37E4H, with bit DØ either set or reset. The following Z-80 assembly language program illustrates how to enable output Ø or output 1.

```
;SELECT CASSETTE OUTPUT ZERO

        LD A , ØØH          ;RESET DØ

        LD (37E4H) , A      ;OUTPUT TO LATCH

;SELECT CASSETTE OUTPUT ONE

        LD A , Ø1H          ;SET DØ

        LD (37E4H) , A      ;OUTPUT TO LATCH
```

The cassette switching circuitry is shown in the lower right corner of sheet 2 of the Expansion Interface schematic. Z40 is a quad NAND gate. It is connected such that it operates like a D latch. Pin 13 of Z40 is the clock input to the latch. Pin 1 of Z40 is the D input and pin 6 of Z40 is the Q output of the latch, A D type latch operates in the following manner: A transistion on the clock input transfers the logic state, currently presented to the D input, to the Q output. Notice from the schematic that the clock input to pin 13 of Z40 is the inversion of the signal, CSW. CSW is generated by writing to memory location 37E4H. Notice also that data bit DØ provides the input to the D latch (pin 1 of Z40). A write to location 37E4H with DØ reset, transfers a logic low to pin 6 of Z40 (the Q output). This logic low is fed to pins 1 and 2 of Z41, which is a high current driver. A low at the inputs to this driver turns off the internal transistor and shuts off the current to the relay coil, thus enabling cassette output Ø. A write to location 37E4H with DØ set, transfers a logic high to pin 6 of Z40 (the Q output). This logic high is fed to pins 1 and 2 of Z41. A high on the inputs to this driver turns on the internal transistor which enables current to flow through the relay coil. This forces the relay to switch states, thus enabling cassette output 1.

EXPANSION INTERFACE RAM

(Refer to Schematic Diagram, Figure 7, Sheet 2)
Address lines AØ – A13 are gated via multiplexers Z17 and Z18 down to the seven address inputs of the 16K Dynamic RAMs. The multiplexer control line MUX is generated by the TRS-80 Microcomputer, as is the write strobe WR* and the row address strobe RAS*.

The multiplexed addresses, WR* and RAS*, are applied to the RAM array. The signals 32K and 48K are generated by the Address Decoder logic, as explained previously in this Manual.

The 16K Dynamic RAMs are "selected" by a logical "Ø" input on pin 15, of RAMs Z9 through Z16, which is the $\overline{CAS}$ input. $\overline{CAS}$*, which is generated by the TRS-80, provides the timing pulse for the column address/chip select. CAS* is ANDed with the 32K and 48K to provide the appropriate RAM decode signal.

LINE PRINTER INTERFACE

The Expansion Interface provides the owner with a parallel printer interface which is compatible with the Radio Shack line of printers. This interface type was chosen because it is a widely used industry standard, is reliable and is easily implemented. The signals related to the printer are available on a 34 pin port, located on the left rear corner of the Expansion Interface. These signals are routed to the printer via a twisted wire pair cable (Part #6000910) that has a 34 pin edge card connector on the Expansion Interface end and a 36 pin D-cinch plug on the printer end.

The printer interface is essentially a latched eight bit output port and a four bit input port with a pulse stretcher for the data strobe input to the Line Printer. This I/O port is accessed by either writing or reading from memory address 37E8H. A write to 37E8H loads the output latches (Z44 and Z45) with the character to be printed and triggers the pulse stretcher (1/2 of Z29). The pulse stretcher provides a 1.5 microsecond low-going strobe which provides timing information to the printer. The rising edge of the data strobe transfers the data from the output latches (Z44 and Z45) to the data buffer internal to the Line Printer.

A read operation from 37E8H reads four bits of status information related to the Line Printer. Each bit (D7 - D4) relates to specific information about the operation of the printer. Bits D3 - DØ are not used.

The Radio Shack Line Printer recognizes two control characters: line feed (ØAH) and carriage return (ØDH). Output of either of these two control codes causes the printer to go busy. "Busy" means that the printer cannot accept any more data until it finishes the operation initiated by the control codes. The printer relays this busy indication by asserting a logic one on its busy output line. This output is routed to bit D7 (pin 6 of Z46) via the Line Printer cable. Z46 is a tri-state buffer which is enabled by reading 37E8H. The buffer, internal to the Line Printer, has a maximum capacity of 132 characters. Filling up this buffer will result in the printer "going busy", the contents being printed and the buffer cleared in anticipation of the next line of characters. Reception of a carriage return causes the contents of the buffer to be printed; busy asserted logic one for the duration of the print; advance of the paper one line and return of the print carriage to the low position. Reception

of a line feed causes an advance of the paper one line; busy asserted logic one for the duration of the advance and clearing of the line buffer.

Paper empty is the other status bit utilized by the Radio Shack Line Printer. This printer output is routed to bit D6 (pin 4 of Z46) via the Line Printer cable. Paper empty is asserted logic one if the paper empty microswitch (on the Line Printer) is opened. Two other status signals are routed to the Expansion Interface (unit select and fault), but are unused by the Radio Shack Line Printer or the Expansion Interface. Paper empty and busy are wire ORed internally by the Line Printer logic. This means that these status bits are not independent. In other words, when busy goes high, paper empty does also. When interfacing to the Radio Shack printer it's therefore necessary to check only one of these two status bits and not both. The following Z-80 assembly language program illustrates how one would output data to the printer:

```
; ASSUME CHARACTER TO BE PRINTED IS IN C

CHSTAT   LD A , (37E8H)      ; LOAD A W/PRINTER
                               STATUS

         BIT 7 , A           ; TEST BIT 7 , BUSY

         JR NZ , CHSTAT      ; LOOP IF NOT LOW

         LD (37E8H) , A      ; OUTPUT TO PRINTER
                               INTERFACE

         RET                 ; RETURN FROM SUB-
                               ROUTINE
```

This subroutine loads the printer status into the A register; tests bit 7 (busy); checks status again if bit 7 is high, or transfers the character to be printed into the A register if bit 7 is low; loads the latches in the printer interface with the character to be printed and returns to the routine that initiated the call.

REAL– TIME CLOCK

The Real-Time Clock (RTC) provides an interrupt (asserted low) every 25 milliseconds at pin 21 of J2. This time period corresponds to 40 Hz. The interrupt (INT) allows programming to count seconds, minutes, etc. for user determined purposes. The programming can be DOS (Disk Operating System) if it is in a disk system or in a user supplied machine program if not.

The 4 MHz oscillator (Z31, Y1, C39, C40, R18 and R19) output is buffered by Z31 (pins 14 and 15) and is divided down in frequency by Z27, Z26 and Z25, producing a 25 millisecond period pulse at pin 3 of Z30. The rising edge of the pulse at pin 3 causes Q (pin 5) to go low, which causes pin 8 of Z30 to go low. This low, through Z35 (pins 9 and 10) and Z23 (pins 12 and 13), sets pin 9 of Z28 (interrupt flip-flop) high, asserting an interrupt request (INTRQ).

The interrupt service routine must read (LD A, (37EØH) instruction) from memory address 37EØH, causing reset of the interrupt latch. Bit 7 of the read-in byte, if equal to 1, indicates that the RTC generated the interrupt request and that a read from 37EØH will not reset the interrupt request latch (Z28, pin 9) unless the Floppy Disk Controller (FDC) is serviced as described elsewhere.

FLOPPY DISK INTERFACE

The FDC (Western Digital FD1771B-01 Large Scale Integrated Circuit) contains most of the logic for controlling the Disk drives. The internal logic of the FDC:

1. keeps account of track number
2. generates error checking codes (CRCs)
3. separates the Disk head output into data
4. scans for identification fields (in contrast to data)
5. does, in general, much of the housekeeping involved in reading and writing data from/to disks.
   (See Appendix A (1771 data sheet))

Communication between the FDC internal registers and the TRS-80 is via the tri-state buffers – Z33, Z37 and Z38 which are controlled by address decoding circuits Z32, Z42 and Z43. The FDC (Z34) also requires the 1 MHz clock square wave input at pin 24. This square wave signal comes from pin 6 of the divide-by-4 counter (Z27 and Z28).

As shown on the schematic, the FDC directly controls the drive motors; track stepping and direction; write gating and data. It also inputs information on the diskette index position, track zero occurrence, write protection and data/clocking – all at J5 on the Expansion Interface. The FDC registers (CMD/STATUS, TRACK, SECTOR, DATA) are located at TRS-80 memory addresses 37ECH, 37EDH, 37EEH and 37EFH, respectively.

Drive selection is through Z36. Only one drive is selected at a time. A time-out timer circuit (Z29) is activated/re-activated each time a drive is selected/re-selected, thereby protecting the disk drives in the instance of program "crashes", as the drives are not designed for continuous motor-on use. After two or three seconds the MOTOR ON line (J5, pin 16) will deactivate (go high) unless Z29 is retriggered by a drive selection/re-selection. Pin 6 of gate Z35 provides a signal to the FDC (pins 23 and 32) when a head load has been commanded (FDC status = READY).

DOS programming takes into account that the Disk drive motor requires one second to come up to operating speed and that head loading takes 80 milliseconds to stabilize. At the end of an FDC operation, an interrupt is generated (pin 39 of the FDC goes high) which, through gate Z35 (pins 12 and 13), sets Z28, pin 9. This interrupt request is terminated by reading the FDC status register (address 37ECH) which makes pin 39 of the FDC go low, then reading from 37EØH which resets pin 9 of Z28.

USER PROGRAMMING OF THE FDC AND RTC

It is intended, due particularly to the complexity of the floppy disk operation, that users and service personnel never need to be concerned with the detailed events involved. User access to the disk subsystem, bypassing TRSDOS, **is not and cannot be supported by Radio Shack and its representatives.** None-the-less, there will be knowledgeable users who will, with the understanding that they are "on their own", make such use of the RTC or Disk. We merely offer the following as sources of information to use as a starting point:

1. The Shugart SA400 OEM and Service manuals

2. The Western Digital FD1771B-01 Data Sheet (included as an appendix to this manual)

In order to use the RTC in a Level II system with the Expansion Interface, but without any disk drives, code can be written in machine language to update a "software clock" if the following is done:

1. An "Interrupt Service Routine" is written which, when called:
   a. Disables the interrupt
   b. increments the software clock counter
   c. reads from the FDC status register (i. e., LD A , (37ECH))
   d. reads from 37EØH (which resets the interrupt latch)
   e. enables the interrupt and returns to the interrupt program:

      EI
      RET

2. The interrupt default link at 4Ø12H, 4Ø13H and 4Ø14H is replaced with a jump to the Service Routine.

3. An EI (enable interrupt) instruction is placed somewhere in the user's main program.

Again, we must emphasize that we cannot support a customer activity in this area. Our cost/price structure simply does not allow it. We could not sell computer equipment at our low prices if we did.

SYSTEM POWER SUPPLY

The TRS-80 needs three voltage levels: +12 volts at about 350 milliamps; +5 volts at about 1.2 amps; and −5 volts at 1 milliamp. The +12 and −5 volts are needed by system RAM, and everything needs +5 volts. The +12 volt and +5 volt supplies are regulated and current protected against shorts. The −5 volt supply is not as critical as the other two supplies and it uses a single zener diode for regulation. Raw, unregulated power is supplied to all regulator circuits from a UL approved "AC adapter".

AC ADAPTER

The AC adapter (or power pack) is a large version of the type used in calculators or TV game products. Inside the plastic case is a single transformer with one primary and two secondary windings. The primary circuit is designed for 115 VAC and has an operating range of 105 to 135 VAC. There is a wire fuse in the primary side to meet UL specifications.

The two secondary circuits are both center tapped. One secondary is rated at 14 volts AC at 1 amp. This circuit is used in the +5 and −5 volt supplies. The other secondary winding uses internal diodes and it outputs 19.8 VDC at about 350 milliamps. This circuit is used in generating the 12 volt supply. All voltage outputs and center taps are brought into the power input at J9.

+12 V POWER SUPPLY

Raw, unregulated voltage for the +12V supply is inputted at pin 2 of J9. When power switch S1 is closed, C47 filters the voltage and the net result is 20 volts or so, applied to Q3 and to regulator Z51. Figure 2 shows a simplified diagram of the internal circuitry in a 723 regulator chip. The illustration will help in the regulator operation discussion.

The filtered DC voltage from the power pack and C47 is applied to pin 12 of Z51 and the emitter of series pass transistor Q3. The voltage applied to pin 12 allows a constant current source to supply zener current for Za. Pin 6 of Z51 will output a zener voltage of about 7.15 volts. Pin 6 is tied to pin 5, the positive input to operational amplifier Zb. The negative input to the op-amp is tied to the wiper of R27. Initially, pin 4 of Z51 is at ground, forcing the output of op-amp Zb to output about 7.15 volts. Transistor Qa turns on, which turns on pass transistor Q3. The pass transistor supplies voltage for current monitoring resistor R8 and to the resistor network R10, R27 and R9. If R27 is adjusted for 7.15 volts at its wiper the op-amp will be balanced and Q3 will output only enough voltage to keep the loop stable. If output voltage decreased below 12 volts, Zb's output would decrease, which would force the current through Qa to decrease. Qa would cause Q3 to increase the current through it and the output would rise back up to the 12 volt level. If the 12 volt line increased in voltage, the op-amp would cause Qa's current to increase, forcing Q3 to slow down.

The transistor labeled Qb in Figure 2, is used to protect power transistor Q3 against over-current damage. If R8 drops sufficient voltage to cause the resistor node at Z51, pin 2, to reach 12.6 volts, Qb will take command of Qa. As Qb is turned on, Qa turns off which starts turning Q3 off. The voltage at Z51, pin 10, must approach 14.7 volts before Qb takes charge of Qa. A voltage of 14.7 at pin 10 of Z51, means that the 12 volt supply is approaching its maximum design current of 480 milliamps. If a short develops across the 12 volt supply, Qb will activate, forcing Qa to

shut down. With Qa off, Q3's base rises to the input voltage level because of R11. Q3 snaps off the supply, preventing it from attempting thermal suicide. Once the short is removed, Qb will turn off and the system will operate normally.

Capacitor C8, connected between pins 13 and 4, is a frequency compensation capacitor. It prevents the op-amp loop from going into oscillation. C9 and C10 are the supply's output filtering and noise suppressing capacitors.

+5 VOLT SUPPLY

The +5 volt power supply also uses a 723 regulator. Due to the current and voltage requirements, more components were stuck around the regulator for support. But the basic circuit operates the same. Figure 2 will also be used in this circuit.

For the +5 volt supply, the AC adapter supplies about 17 volts AC at J9, pins 1 and 3. Full-wave rectifier, CR4, rectifies the AC. When S1 is closed, about 7 VDC is passed through the switch contacts and is filtered by C5.

The power supply for Z50 and the current source for zener Za is taken from the regulated side of R8 in the 12 volt section. Pin 7 is grounded as in Z51 but the zener output is handled differently. The 7.15 volt zener voltage is applied to the resistor network consisting of R7, R26 and R6. When R26 has been adjusted for a 5 volt output on the supply bus, pin 5 of Z50 will be at about 5 volts. The negative input of the op-amp, Zb, is tied to the 5 volt bus. The op-amp controls Qa, which controls bias drive for Q2. Q2 is used to handle the greater base drive necessary for pass transistor Q4. Q4's collector is tied to current sensing resistor R5. R5 monitors the current that the 5 volt bus is producing just as R8 does for the 12 volt bus.

Circuit operation is exactly the same for Z50 as it was for Z51. If op-amp Zb detects a rising or falling voltage condition at the output bus, it will adjust base current to Qa. Since Qa cannot handle the drive requirements for Q1 directly, Q2 is needed for current gain. During a current limiting condition, Qb monitors the voltage access, R5, which is a direct function of bus current. As Qb begins to turn on, it will start sinking current away from the base of Qa. As Qb takes command of the regulator loop, Qa is commanded to start cutting Q2 off. Q2 begins to turn Q1 off and the circuit goes into current limiting. The current limiting action of Qb starts to come into play when the voltage across R5 approaches 0.6 volt. Ohm's Law tells us that the bus current at this voltage level is approaching 1.82 amps.

C1, connected between pins 13 and 4 of Z50, performs the same compensation function as C8 of Z51. C2 and C3 are the output filtering and noise suppressing capacitors while the 0.1 microfarad capacitors are distributed all over the Board to suppress transient spikes. Notice zener diode CR3 on the 5 volt bus. This diode is used as crowbar circuit protection in case of catastrophic failure in the RAMs. If something happens in the system RAM circuit that causes a short between the 12 and 5 volt buses, CR3 would turn on, causing the 5 volt bus to go into current limiting. Since CR3 is a 6.2 volt zener, it would protect the TTL devices that are connected to the 5 volt bus from being damaged by a sudden 12 volt supply voltage. Normally, CR3 would be off with no current flowing through it.

Notice one item: The 12 volt supply must be working properly before the 5 volt supply will operate correctly. Therefore, the 12 volt supply must be adjusted before the 5 volt supply.

–5 VOLT SUPPLY

Source voltage for the –5 volt supply comes from the negative terminal of rectifier CR4. When switch S1 is closed, the negative DC is filtered by C1 and about –11 volts is applied to resistor R4. R4 is used to limit current for zener regulator CR1, a 5.1 volt device. The –5 volt circuit is about as simple a power supply as can be designed. C7 and C6 are the –5 volt supply output filtering and noise suppressing capacitors while C19 through C26 perform the transient suppression function.

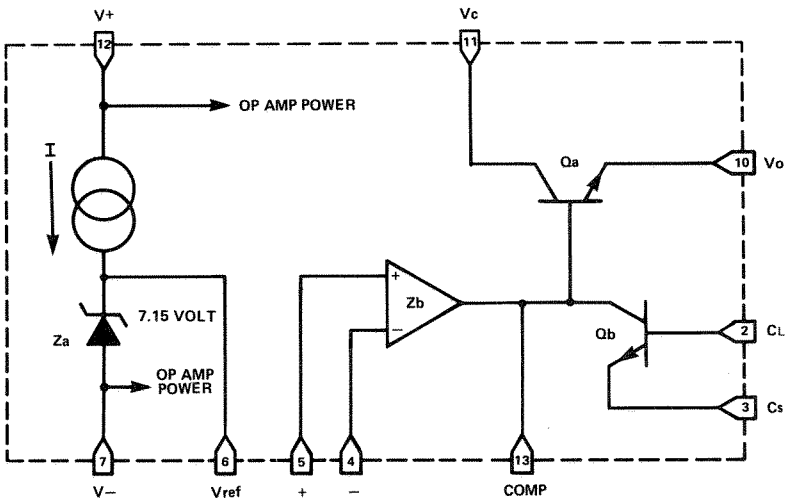


FIGURE 2. BLOCK DIAGRAM OF 723 REGULATOR

POWER SUPPLY CHECKS AND ADJUSTMENTS

Once the unit has been removed from the plastic case and the Board is resting on the test bench, connect the power DIN plug.

CAUTION

The Expansion Interface Board is now "upside down" in reference to its normal position in the case. Be sure you insert the power DIN plug in the power jack, J9 and not in the Cassette jacks (J6, J7, J8). The power jack is the one closest to the large heat sink.

Turn on power to the Expansion Interface Board and test the power supply voltages (see Figure 5):

1. Attach a digital voltmeter or equivalent, with the common (–) lead to the top side of capacitor, C5 – that's the largest capacitor on the Board.

2. **12 VOLT SUPPLY.** Select the +20 volt DC scale on the meter and touch the red (+) lead to the bottom side of the power resistor, R8. (The "bottom side" is the end closest to capacitor C5). Voltage should read 12.0 volts ±5% (12.6 to 11.4 volts). If the voltage does not fall within these limits, adjust resistor R27 for a correct reading (R27 is located at the top left corner of the Board).

3. **+5 VOLT SUPPLY.** Select the +10 volt DC scale on the meter and touch the red (+) lead to the left side of capacitor C51 (C51 is located to the right of the large heat sink). Voltage should read 5.0 volts ±5% (5.25 to 4.75 volts). If the voltage does not fall within these limits, adjust resistor R26 for a correct reading (R26 is located just above capacitor C5).

NOTE

Do not attempt a 5 volt supply adjustment unless the 12 volt supply has been checked and is within tolerance.

4. **–5 VOLT SUPPLY.** Select the –10 volt DC scale on the meter and touch the red (+) lead to the anode side of CR1 (CR1 is located directly below capacitor C51). Voltage should read –5 volts ±5%. There is no adjustment for the –5 volt power supply. If this supply fails to fall within the voltage range, you must isolate the problem to a defective component(s).

INTERNAL EXPANSION AREA

The Internal Expansion area has been provided to allow for the addition of an internal printed circuit board within the Expansion Interface — such as the Radio Shack RS-232 Serial Interface.

The Internal Expansion area is accessed by removing the four screws that secure the Expansion area cover in place. Upon removing the cover, the Internal Expansion connector (fastened to the Expansion Interface P. C. Board) can be seen. This connector has the TRS-80 Data Lines (DØ - D7); some of the TRS-80 Address Lines (AØ - A2); the I/O strobes (IN* and OUT*); the reset line SYSRES*; +5 volts; ground; the interrupt line INT* and a decoded signal called E8*.

E8* goes to a logical "Ø" when A3, A5, A6 and A7 are logical "1" and A4 is logical "Ø".

The connector also has connections to Expansion Board Card Edge, J1. These lines allow signals outside the Expansion Interface to be brought up to the Internal Expansion area.

The Expansion Interface "Add-on" Board outline dimensions are shown in Figure 3 and the connections are listed in Table 3.

Internal Connector Pinout for the Expansion Interface "Add-on" Board.

PIN No.	SIGNAL	PIN No.	SIGNAL
1	J1-40	22	A2
2	J1-38	23	IN*
3	J1-36	24	INT*
4	J1-34	25	D1
5	J1-32	26	D2
6	J1-30	27	D3
7	J1-28	28	DØ
8	J1-26	29	AØ
9	J1-24	30	A1
10	J1-22	31	D5
11	J1-20	32	D4
12	J1-18	33	SYSRES*
13	J1-16	34	D7
14	J1-14	35	D6
15	J1-12	36	E8*
16	J1-10	37	NC
17	NC	38	NC
18	NC	39	+5 VDC
19	NC	40	+5 VDC
20	NC	41	GROUND
21	OUT*	42	GROUND

NC=No Connection

TABLE 3

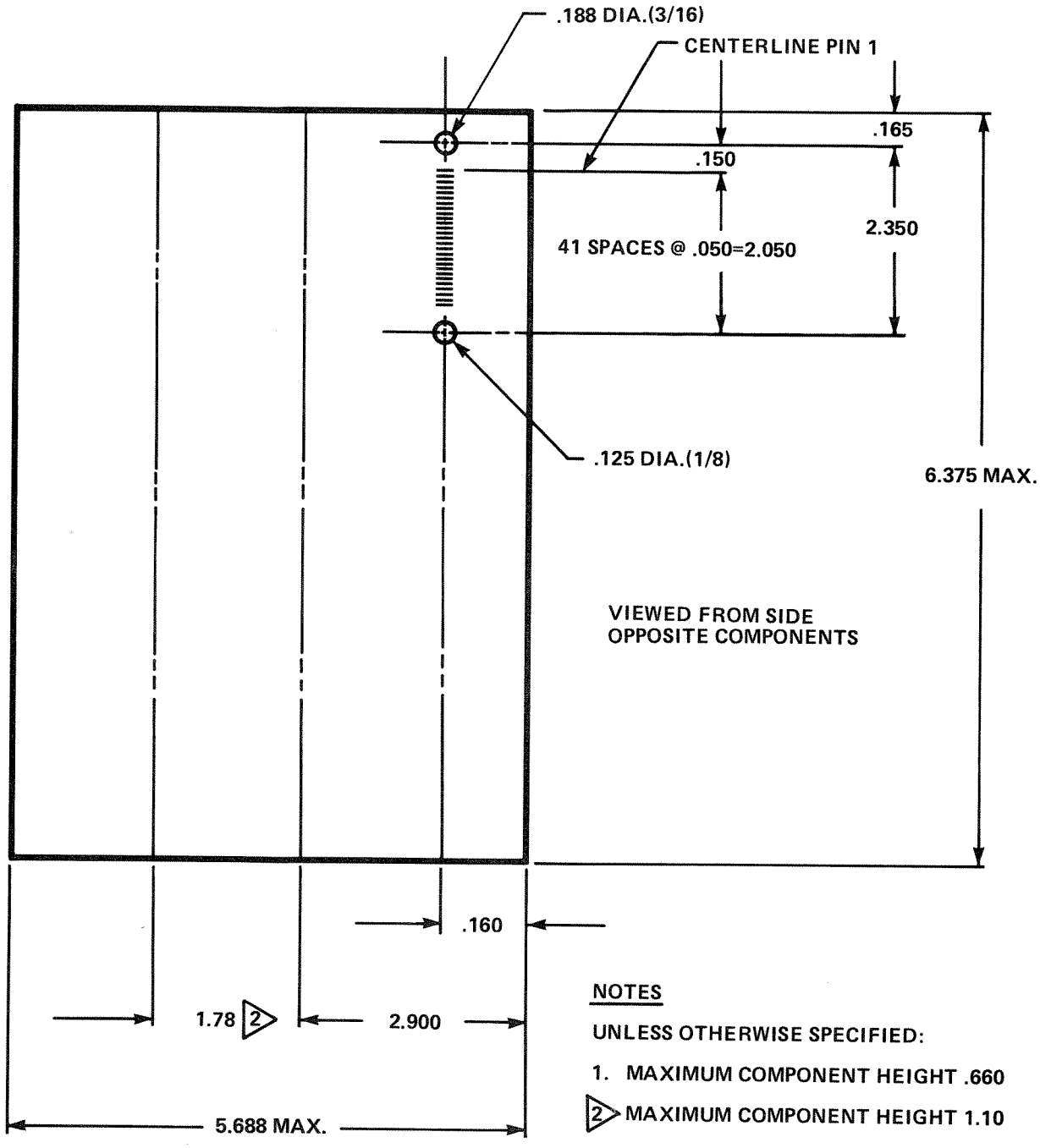


FIGURE 3. EXPANSION INTERFACE "ADD-ON" BOARD OUTLINE DIMENSIONS

EXPANSION INTERFACE
PARTS LIST

SYMBOL	DESCRIPTION	PART NUMBER
	ELECTRICAL	
	PRINTED CIRCUIT BOARD, EXPANSION INTERFACE	1700077
	CAPACITORS	
C1	0.001 μF, 100V, Polyester, Film	1500073
C2	10 μF, 16V, Electrolytic, Radial	1500012
C3	0.01 μF, 25V, Ceramic, Disc	1500047
C4	220 μF, 16V, Electrolytic, Radial	1500069
C5	10,000 μF, 16V, Electrolytic Axial	1500058
C6	0.01 μF, 25V, Ceramic, Disc	1500047
C7	10 μF, 16V, Electrolytic, Radial	1500012
C8	0.001 μF, 100V, Polyester, Film	1500073
C9	0.01 μF, 25V, Ceramic, Disc	1500047
C10	10 μF, 16V, Electrolytic, Radial	1500012
C11	0.1 μF, 50V, Ceramic, Disc	1500053
C12	0.1 μF, 50V, Ceramic, Disc	1500053
C13	0.1 μF, 50V, Ceramic, Disc	1500053
C14	0.1 μF, 50V, Ceramic, Disc	1500053
C15	0.1 μF, 50V, Ceramic, Disc	1500053
C16	0.1 μF, 50V, Ceramic, Disc	1500053
C17	0.1 μF, 50V, Ceramic, Disc	1500053
C18	0.1 μF, 50V, Ceramic, Disc	1500053
C19	0.1 μF, 12V, Ceramic, Disc	1500052
C20	0.1 μF, 12V, Ceramic, Disc	1500052
C21	0.1 μF, 12V, Ceramic, Disc	1500052
C22	0.1 μF, 12V, Ceramic, Disc	1500052
C23	0.1 μF, 12V, Ceramic, Disc	1500052
C24	0.1 μF, 12V, Ceramic, Disc	1500052
C25	0.1 μF, 12V, Ceramic, Disc	1500052
C26	0.1 μF, 12V, Ceramic, Disc	1500052
C27	0.1 μF, 50V, Ceramic, Disc	1500053
C28	0.1 μF, 50V, Ceramic, Disc	1500053
C29	0.1 μF, 50V, Ceramic, Disc	1500053
C30	0.1 μF, 50V, Ceramic, Disc	1500053
C31	0.1 μF, 50V, Ceramic, Disc	1500053
C32	0.1 μF, 50V, Ceramic, Disc	1500053
C33	0.1 μF, 50V, Ceramic, Disc	1500053
C34	0.1 μF, 50V, Ceramic, Disc	1500053
C35	0.1 μF, 12V, Ceramic, Disc	1500052
C36	0.1 μF, 12V, Ceramic, Disc	1500052
C37	0.1 μF, 12V, Ceramic, Disc	1500052
C38	0.1 μF, 12V, Ceramic, Disc	1500052
C39	10 pF, 50V, Ceramic, Disc	1500067
C40	75 pF, 50V, Ceramic, Disc	1500068
C41	0.1 μF, 12V, Ceramic, Disc	1500052
C42	0.1 μF, 12V, Ceramic, Disc	1500052
C43	0.1 μF, 12V, Ceramic, Disc	1500052
C44	0.1 μF, 12V, Ceramic, Disc	1500052
C45	0.1 μF, 12V, Ceramic, Disc	1500052
C46	0.1 μF, 12V, Ceramic, Disc	1500052
C47	2,200 μF, 35V, Electrolytic, Axial	1500064
C48	33 μF, 6.3V, Electrolytic, Radial	1500065
C49	10 μF, 16V, Electrolytic, Radial	1500012
C50	0.1 μF, 12V, Ceramic, Disc	1500052
C51	47 μF, 16V, Electrolytic, Axial	1500075
C52	47 μF, 16V, Electrolytic, Axial	1500075
C53	33 μF, 16V, Electrolytic, Radial	1500074
C54	Not Used	
C55	10 μF, 16V, Electrolytic, Radial	1500012
C56	33 μF, 16V, Electrolytic, Radial	1500074
C57	33 μF, 16V, Electrolytic, Radial	1500074
C58	33 μF, 16V, Electrolytic, Radial	1500074
C59	33 μF, 16V, Electrolytic, Radial	1500074
C60	Not Used	
C61	0.1 μF, 12V, Ceramic, Disc	1500052
C62	0.1 μF, 12V, Ceramic, Disc	1500052
C63	0.1 μF, 12V, Ceramic Disc	1500052
C64	200 pF, 50V, Ceramic, Disc	1500066
C65	47 μF, 16V, Electrolytic, Axial	1500075
C66	Not Used	
C67	200 pF, 50V, Ceramic, Disc	1500066
	DIODES	
CR1	1N5231, 5.1V, Zener, Selected	4800022
CR2	1N4148, Silicon	4800002
CR3	1N4735, 6.2V, Zener	4800021
CR4	MDA202, 2A, 200V, Bridge Rectifier	4800023
	JACKS	
J6	Connector, Socket, DIN, 5-Pin	2100033
J7	Connector, Socket, DIN, 5-Pin	2100033
J8	Connector, Socket, DIN, 5-Pin	2100033
J9	Connector, Socket, DIN, 5-Pin	2100033
	RELAYS	
K1	5V, 4PDT	4500002
	TRANSISTORS	
Q1	MJE2955, Power, PNP	4824005
Q2	2N3904, General Purpose, NPN	4822001
Q3	MJE2955, Power, PNP	4824005

EXPANSION INTERFACE
PARTS LIST (Cont'd)

SYMBOL	DESCRIPTION	PART NUMBER
	RESISTORS	
R1	560 ohm, 1/4 W, 5%	4704041
R2	4.7K, 1/4 W, 5%	4704061
R3	68 ohm, 1/2 W, 5%	4708022
R4	220 ohm, 1/2 W, 5%	4708032
R5	0.33 ohm, 2 W, 5%	4717004
R6	3.3K, 1/4 W, 5%	4704058
R7	1.2K, 1/4 W, 5%	4704049
R8	5.6 ohm, 3 W, 5%	4717003
R9	3.3K, 1/4 W, 5%	4704058
R10	2.2K, 1/4 W, 5%	4704054
R11	1.2K, 1/4 W, 5%	4704049
R12	2K, 1/4 W, 5%	4704053
R13	12K, 1/4 W, 5%	4704070
R14	150 ohm, 1/4 W, 5%	4704028
R15	200K, 1/4 W, 5%	4704091
R16	20K, 1/4 W, 5%	4704073
R17	4.7K, 1/4 W, 5%	4704061
R18	1K, 1/4 W, 5%	4704047
R19	15 MEG, 1/4 W, 5%	4704127
R20	10K, 1/4 W, 5%	4704068
R21	10K, 1/4 W, 5%	4704068
R22	150 ohm, 1/4 W, 5%	4704028
R23	150 ohm, 1/4 W, 5%	4704028
R24	150 ohm, 1/4 W, 5%	4704028
R25	10K, 1/4 W, 5%	4704068
R26	1K, 30%, Variable	4750019
R27	1K, 30%, Variable	4750019
R28	2.2K, 1/4 W, 5%	4704054
R29	4.7K, 1/4 W, 5%	4704061
R30	4.7K, 1/4 W, 5%	4704061
R31	4.7K, 1/4 W, 5%	4704061
R32	4.7K, 1/4 W, 5%	4704061
R33	4.7K, 1/4 W, 5%	4704061
R34	4.7K, 1/4 W, 5%	4704061
R35	150 ohm, 1/4 W, 5%	4704028
	SWITCHES	
S1	4PDT, Push	5102008
	Knob	2500037
	SOCKETS	
X1	16-Pin, I. C. Socket	2100037
X2	16-Pin, I. C. Socket	2100037
X3	16-Pin, I. C. Socket	2100037
X4	16-Pin, I. C. Socket	2100037
X5	16-Pin, I. C. Socket	2100037
X6	16-Pin, I. C. Socket	2100037
X7	16-Pin, I. C. Socket	2100037
X8	16-Pin, I. C. Socket	2100037
X9	16-Pin, I. C. Socket	2100037
X10	16-Pin, I. C. Socket	2100037
X11	16-Pin, I. C. Socket	2100037
X12	16-Pin, I. C. Socket	2100037
X13	16-Pin, I. C. Socket	2100037
X14	16-Pin, I. C. Socket	2100037
X15	16-Pin, I. C. Socket	2100037
X16	16-Pin, I. C. Socket	2100037
X34	40-Pin, I. C. Socket	2100035
	CRYSTALS	
Y1	4.0000 MHz	2300005
	INTEGRATED CIRCUITS	
Z17	74LS157, Quad 2-Line to 1-Line Data Selector/Multiplexer	3102020
Z18	74LS157, Quad 2-Line to 1-Line Data Selector/Multiplexer	3102020
Z19	74LS367, Hex Bus Driver, Non-Inverted Data Output, 3-state	3102024
Z20	74LS00, Quad 2-Input Positive-NAND Gate	3102006
Z21	74LS367, Hex Bus Driver, Non-Inverted Data Output, 3-state	3102024
Z22	74LS367, Hex Bus Driver, Non-Inverted Data Output, 3-state	3102024
Z23	74LS04, Hex Inverter	3102008
Z24	74LS32, Quad 2-Input Positive OR Gate	3102014
Z25	4518, Dual BCD Up Counter	3102034
Z26	4518, Dual BCD Up Counter	3102034
Z27	74LS90, Decade Counter	3102031
Z28	74LS74, Dual D Positive-Edge-Triggered Flip-Flop with Preset and Clear	3102015
Z29	74LS123, Dual Retriggerable Mono-stable Multivibrator with Clear	3102033
Z30	74LS74, Dual D Positive-Edge-Triggered Flip-Flop with Preset and Clear	3102015
Z31	4049B, Hex Inverter/Buffer	3102035
Z32	74LS155, Dual 2-Line to 4-Line Decoder/Multiplexer	3102029
Z33	74LS368, Hex Bus Driver	3102025
Z34	FD1771B-01, Floppy Disc Controller	3110002
Z35	74LS20, Dual 4-Input NAND Gate	3102011
Z36	74LS175, Quad D Flip-Flop with Clear	3102023

EXPANSION INTERFACE
PARTS LIST (Cont'd)

SYMBOL	DESCRIPTION	PART NUMBER
Z37	74LS368, Hex Bus Driver, Inverted Data Output, 3-state	3102025
Z38	74LS368, Hex Bus Driver, Inverted Data Output, 3-state	3102025
Z39	7438, Quad 2-Input Positive-NAND Buffer with Open Collector Outputs	3102032
Z40	74LS00, Quad 2-Input Positive-NAND Gate	3102006
Z41	75452, Dual Peripheral Positive-NAND Driver	3106002
Z42	74LS30, 8-Input Positive-NAND Gate	3102013
Z43	74LS139, Decoder/Multiplexer	3102030
Z44	74LS175, Quad D Flip-Flop with Clear	3102023
Z45	74LS175, Quad D Flip-Flop with Clear	3102023
Z46	74LS367, Hex Bus Driver, Non-Inverted Data Output, 3-state	3102024
Z47	7438, Quad 2-Input Positive-NAND Buffer with Open Collector Outputs	3102032
Z48	7438, Quad 2-Input Positive-NAND Buffer with Open Collector Outputs	3102032
Z49	74LS30, 8-Input Positive-NAND Gate	3102013
Z50	723 DIP, Voltage Regulator	3100001
Z51	723 DIP, Voltage Regulator	3100001

ITEM	DESCRIPTION	PART NUMBER
	MECHANICAL	
1	Assembly, TRS-80 Interface Board	7000086
2	Bumper	2800035
3	Case, Lower	1400082
4	Case, Top	1400211
5	Connector, 42 Pin Contact w/mounting hardware	2100046
6	Door, Connector, Expansion Unit 34 Pin	1400212
7	Door, Connector, Expansion Unit 40 Pin	1400216
8	Door, Power Supply, Expansion Unit	1400209
9	Door, PWB, Expansion Unit	1400210
10	Floor, Transformer, Expansion Unit	1400215
11	Screw, Machine (2-56)	2810108
12	Screw, Machine (6-32 x 3/8)	2819356
13	Screw, Machine (6-32 x 1-3/4)	2810624
14	Screw, Machine (6-32 x 2)	2810632
15	Screw, Thread Forming (6-20 x 3/8)	2839696
16	Screw, Thread Forming (6-20 x 1-1/4)	2830620
17	Washer, Flat, #2	2851202
	MISCELLANEOUS	
	*Assembly, Cable, TRS-80 Interface	7000094
	Bracket, Switch	2800038
	*Cable, Audio DIN to Audio DIN	6000909
	*Cable, Audio DIN to Cassette (2)	6000905
	*Hood, Connector, 34 Pin (2)	1400213
	*Hood, Connector, 40 Pin (2)	1400218
	*Hood, TRS-80 Interface Port	1400214
	*Hood, TRS-80 Port	1400217
	Knob, Switch	2500037
	Nut, Hex, Machine, 4-40 (2)	2870005
	*Power Supply, Transformer 105 V to 135 VAC, 60 Hz	4000004
	Screw, Machine, 4-40 (2)	2810212
	Washer, Flat, #4 (2)	2851201

* See Operator's Manual

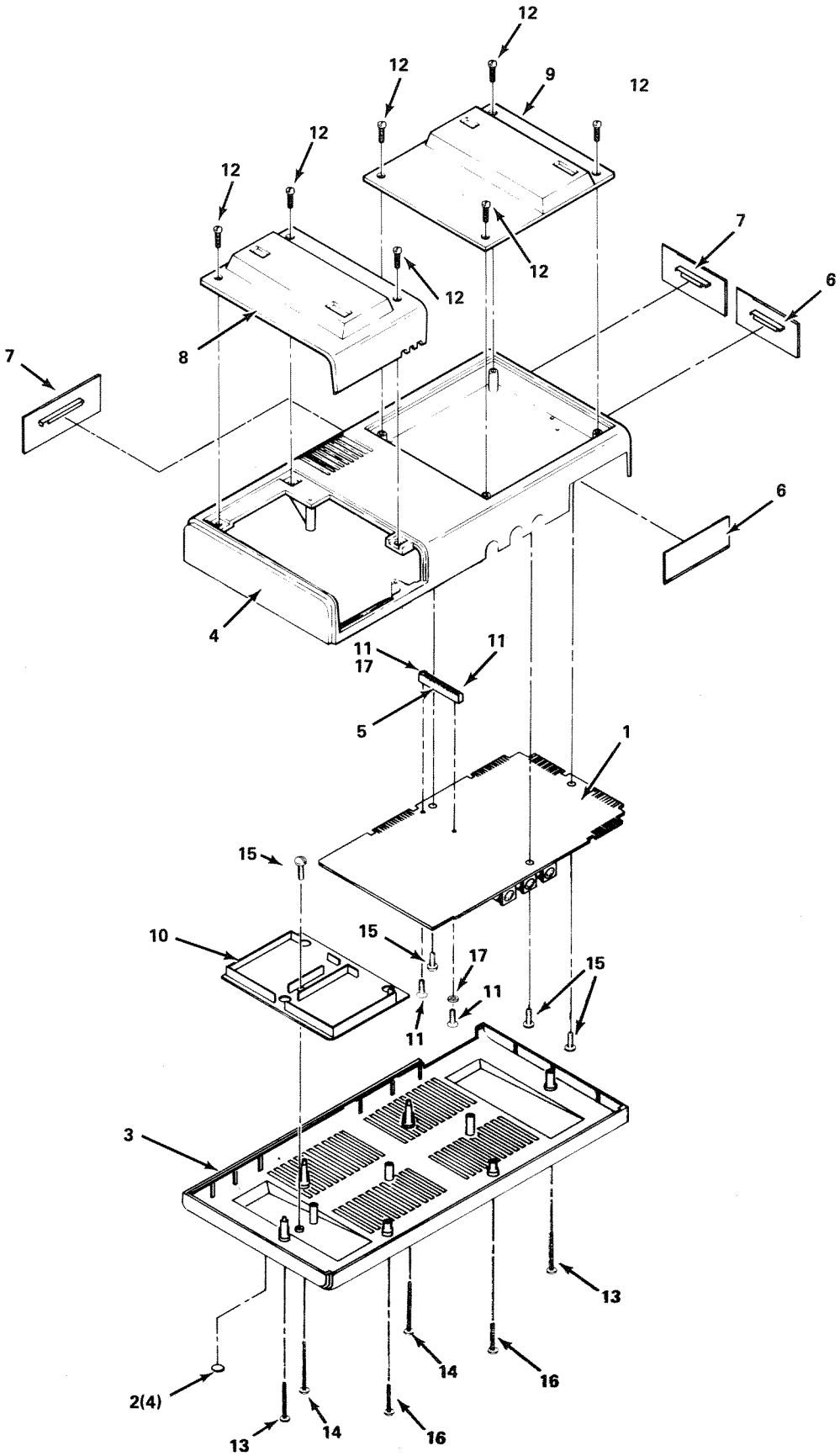


FIGURE 4. EXPLODED VIEW OF THE EXPANSION INTERFACE

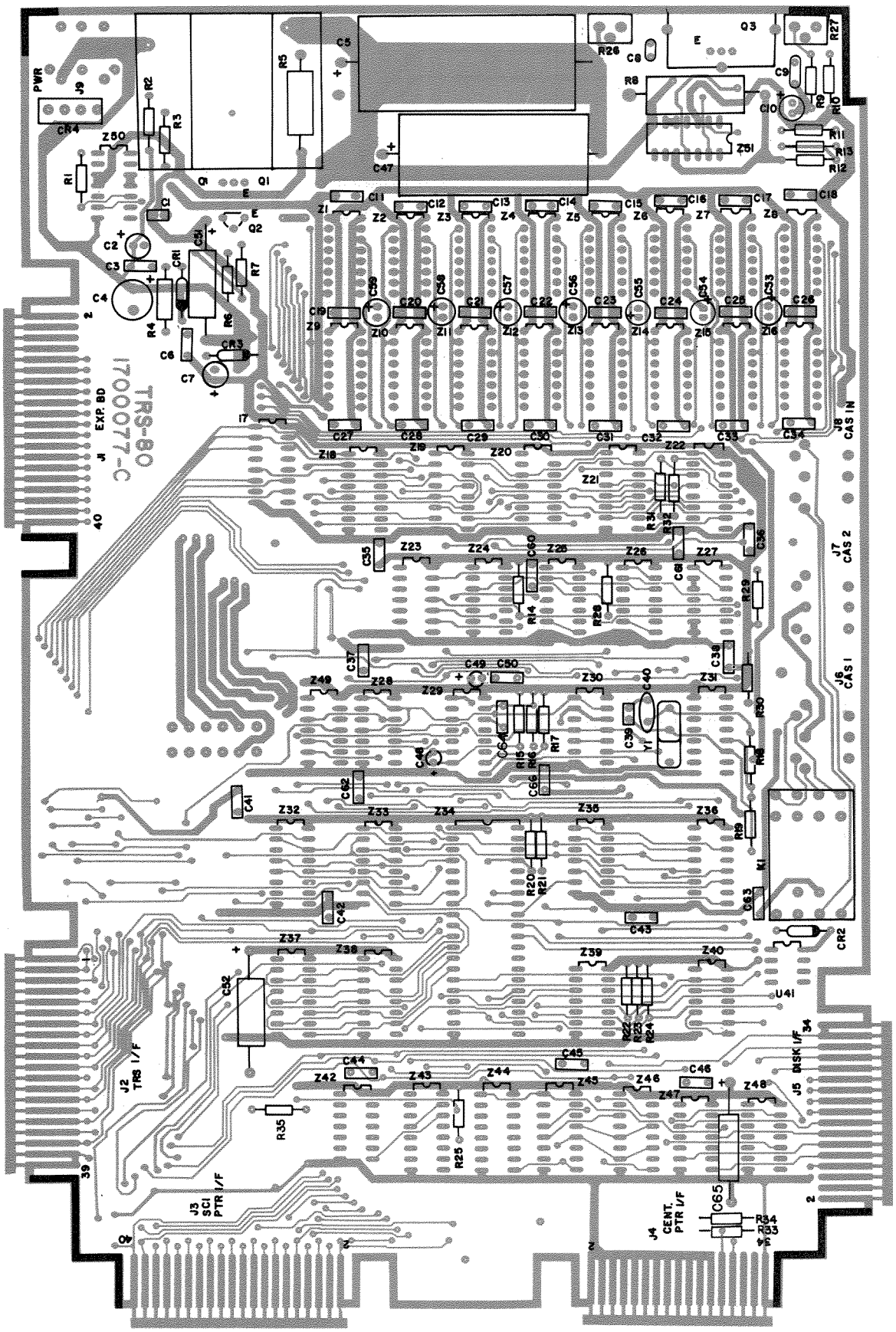


FIGURE 5. EXPANSION INTERFACE P.C. BOARD (TOP VIEW)

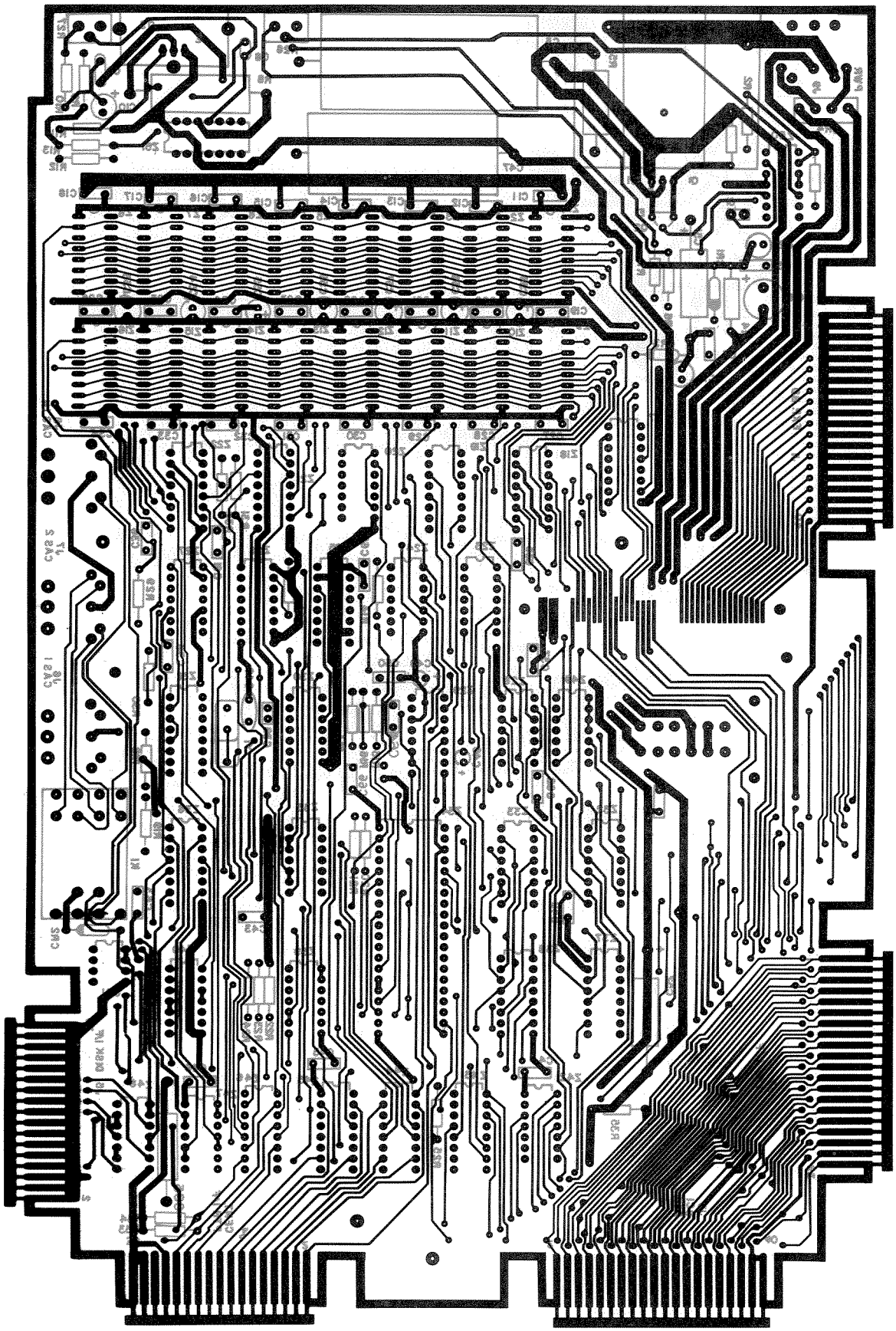
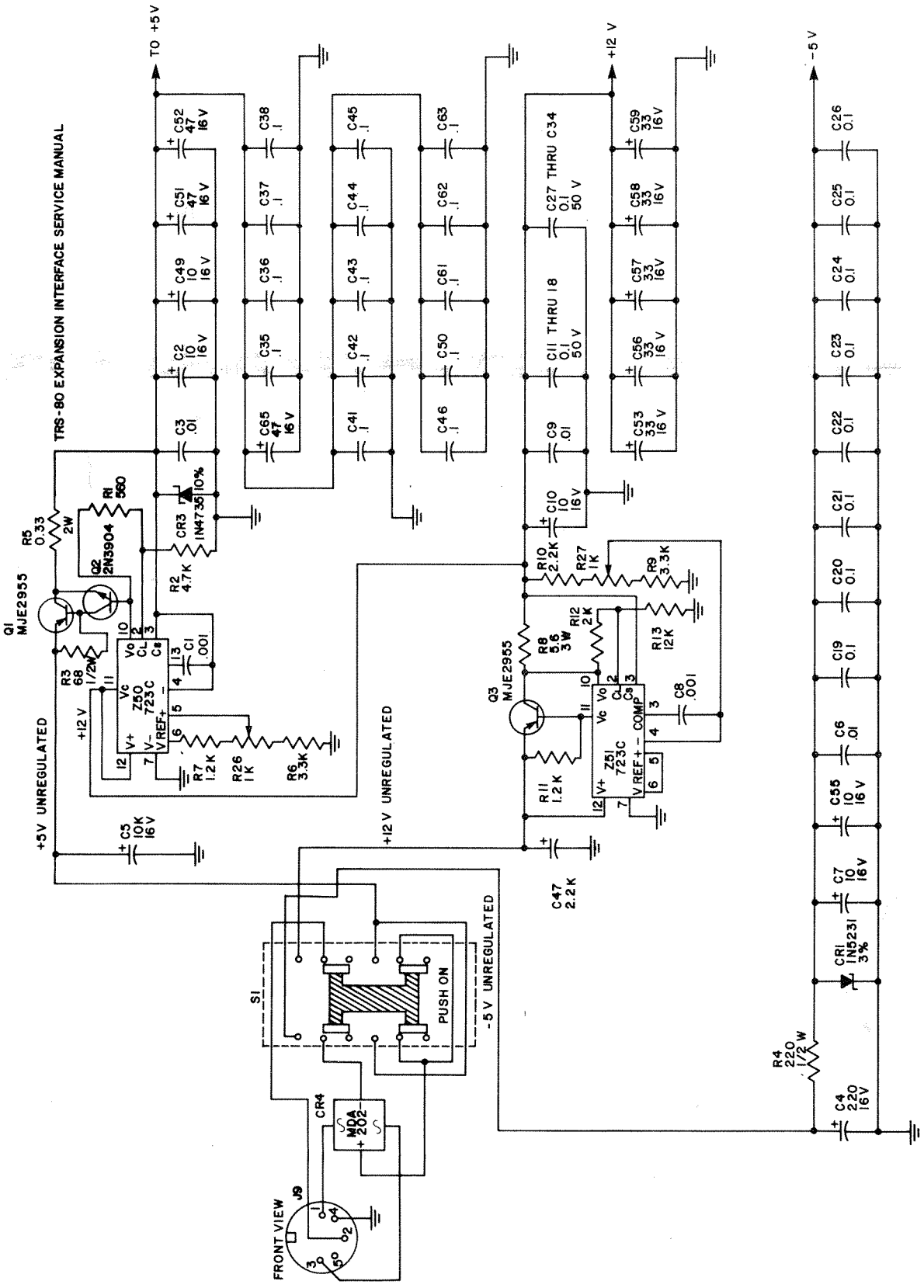
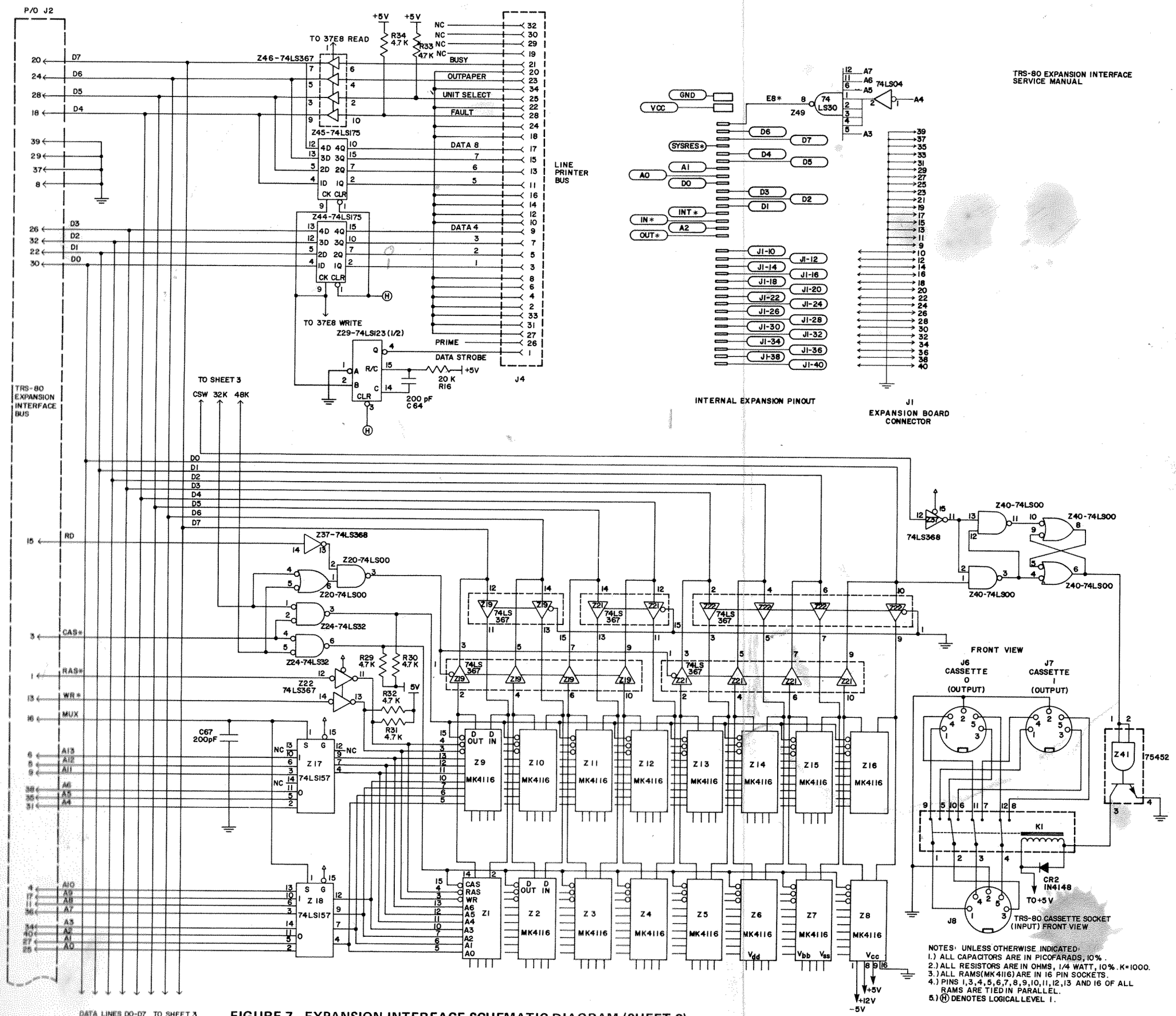


FIGURE 6. EXPANSION INTERFACE P.C. BOARD (BOTTOM VIEW)



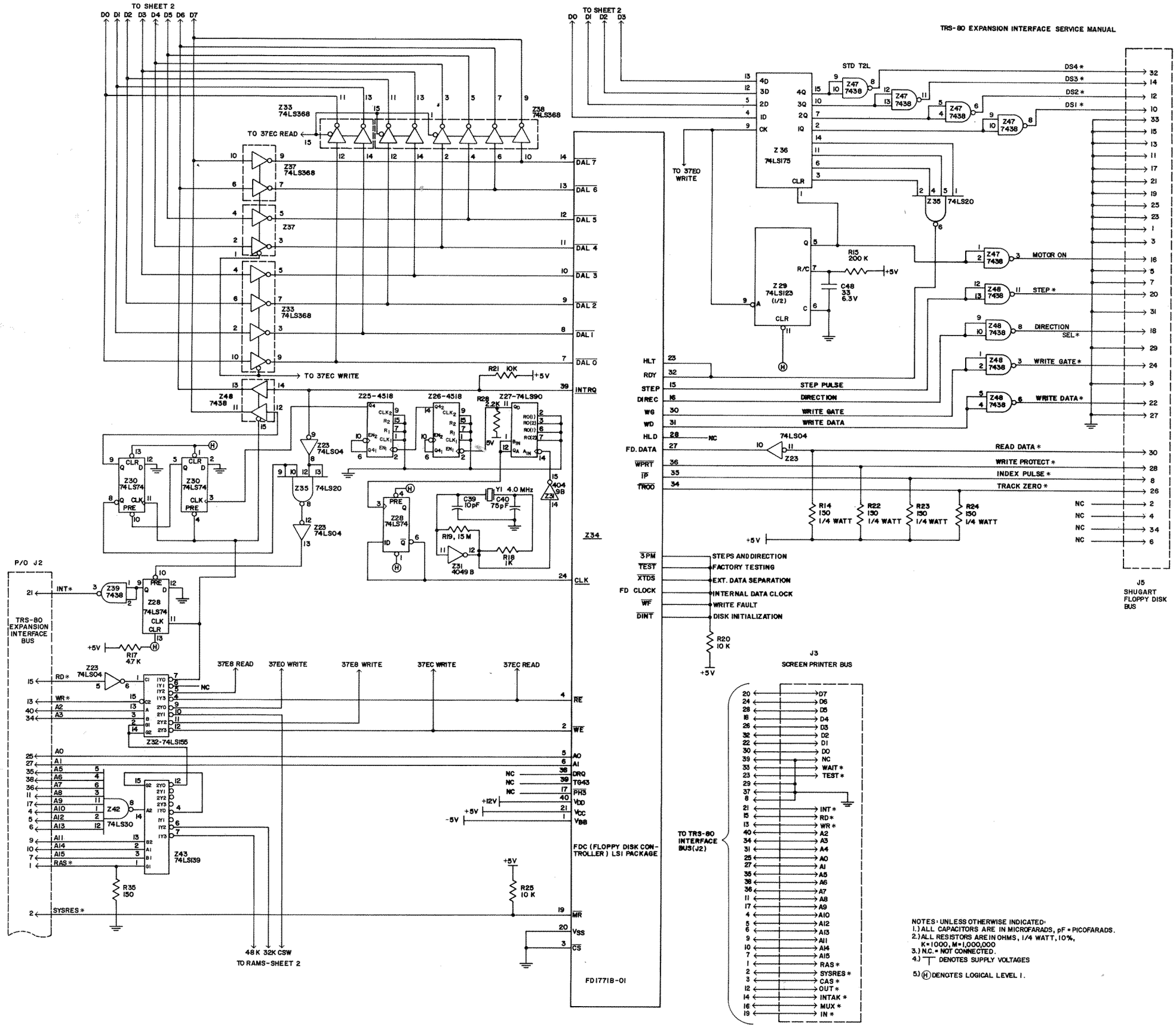
NOTES: UNLESS OTHERWISE INDICATED:
1.) ALL CAPACITORS ARE IN MICROFARADS, K=1000.
2.) ALL RESISTORS ARE IN OHMS, 1/4 WATT, 5%. K=1000.

FIGURE 7. EXPANSION INTERFACE SCHEMATIC DIAGRAM (SHEET 1)



NOTES: UNLESS OTHERWISE INDICATED:
1.) ALL CAPACITORS ARE IN PICOFARADS, 10%.
2.) ALL RESISTORS ARE IN OHMS, 1/4 WATT, 10%. K=1000.
3.) ALL RAMS(MK4116) ARE IN 16 PIN SOCKETS.
4.) PINS 1,3,4,5,6,7,8,9,10,11,12,13 AND 16 OF ALL RAMS ARE TIED IN PARALLEL.
5.) Ⓗ DENOTES LOGICAL LEVEL 1.

FIGURE 7. EXPANSION INTERFACE SCHEMATIC DIAGRAM (SHEET 2)



NOTES: UNLESS OTHERWISE INDICATED:
1.) ALL CAPACITORS ARE IN MICROFARADS, pF = PICOFARADS.
2.) ALL RESISTORS ARE IN OHMS, 1/4 WATT, 10%,
K = 1000, M = 1,000,000
3.) N.C. = NOT CONNECTED.
4.) ⊤ DENOTES SUPPLY VOLTAGES
5.) (H) DENOTES LOGICAL LEVEL 1.

FIGURE 7. EXPANSION INTERFACE SCHEMATIC DIAGRAM (SHEET 3)

WESTERN DIGITAL MOS/LSI APPENDIX FD1771 A/B - 01 - 11

DATA SHEET — FLOPPY DISK FORMATTER/CONTROLLER

MARCH 1978

GENERAL DESCRIPTION

The FD1771 is a MOS/LSI device that performs the functions of a Floppy Disk Controller/Formatter. The device is designed to be included in the disk drive electronics, and contains a flexible interface organization that accomodates the interface signals from most drive manufactures. The FD1771 is compatible with the IBM 3740 data entry system format.

The processor interface consists of a 8-bit bi-directional bus for data, status, and control word transfers. The FD1771 is set up to operate on a multiplexed bus with other bus-oriented devices.

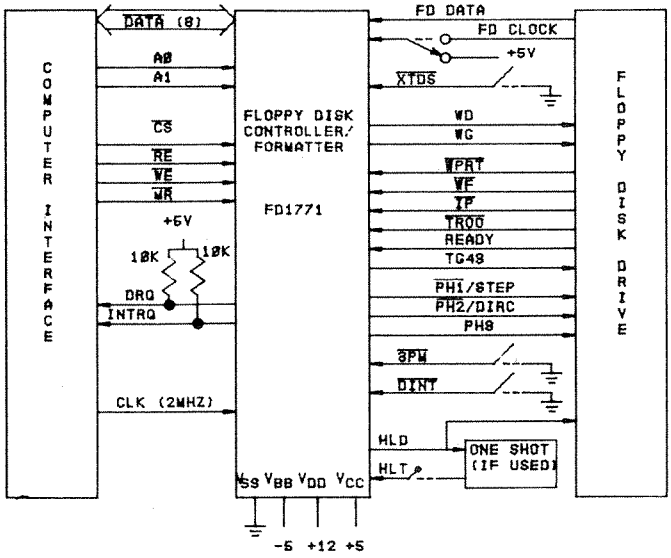
The FD1771 is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs.

APPLICATIONS

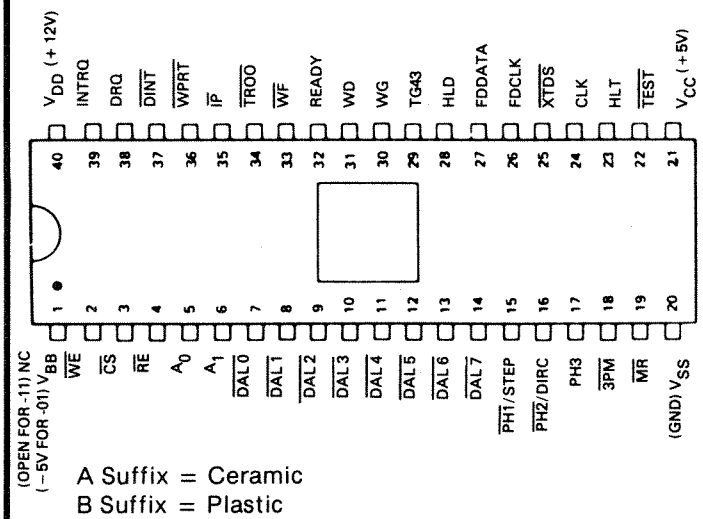
- o FLOPPY DISK DRIVE INTERFACE
- o SINGLE OR MULTIPLE DRIVE CONTROLLER/FORMATTER
- o NEW MINI-FLOPPY CONTROLLER

FEATURES

- o SOFT SECTOR FORMAT COMPATIBILITY
- o AUTOMATIC TRACK SEEK WITH VERIFICATION
- o READ MODE
  - Single/Multiple Record Read with Automatic Sector Search or Entire Track Read
  - Selectable 128 Byte or Variable Length Record
- o WRITE MODE
  - Single/Multiple Record Write with Automatic Sector Search
  - Entire Track Write for Diskette Initialization
- o PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Selectable Head Settling and Head Engage Times
  - Selectable Three Phase or Step and Direction and Head Positioning Motor Controls
- o SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
- o No — 5VDC Power Supply Required on – 11 version



FD1771 SYSTEM BLOCK DIAGRAM
FIG 1



A Suffix = Ceramic
B Suffix = Plastic

FD1771 PIN CONNECTIONS
FIG 2

WESTERN DIGITAL CORPORATION

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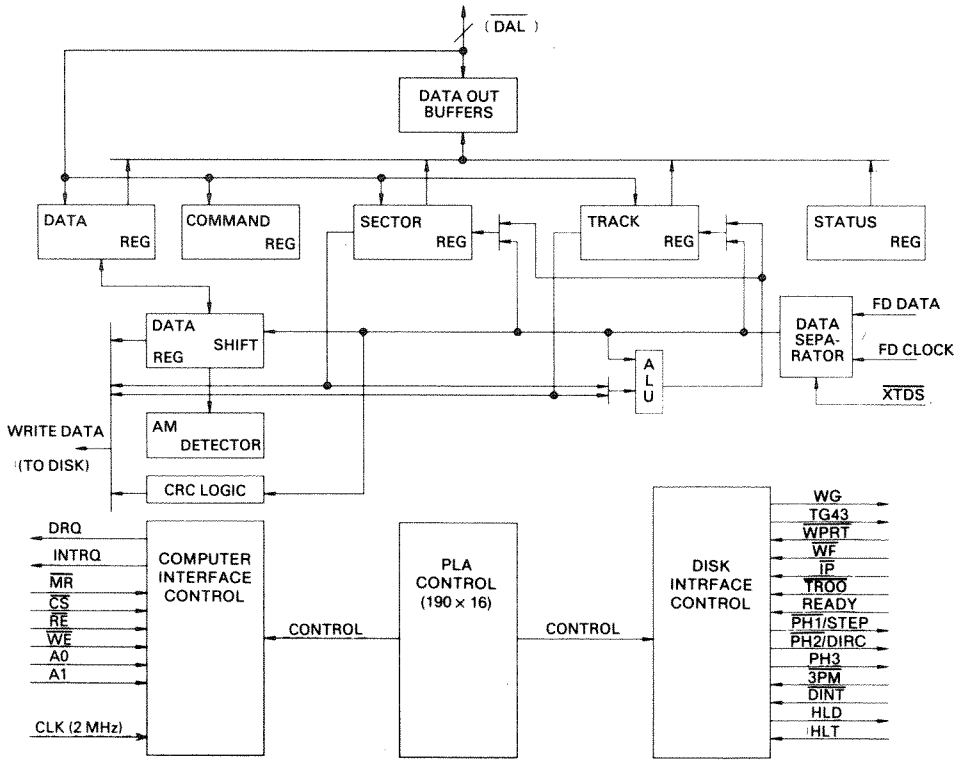
(714) 557-3550 TWX 910-595-1139



FD1771 BLOCK DIAGRAM
FIG 3

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on Page 2. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register - This 8-bit register assembles serial data from the Read Data input (FDDATA) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register - This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register can be loaded from the DAL and gated onto the DAL under processor control.

Track Register - This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when this device is busy.

Sector Register (SR) - This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) - This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) - This 8-bit register holds device Status information. The meaning of the Status bits are a function of the contents of the Command Register. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) - The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

AM Detector - The Address Mark detector is used to detect ID, Data, and Index address marks during Read and Write operations.

Timing and Control - All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from a 2.0 MHz external crystal clock.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD1771. The DAL are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The least-significant address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1-AØ		READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
Ø	Ø	Status Register	Command Register
Ø	1	Track Register	Track Register
1	Ø	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD1771 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

The Lost Data bit and certain other bits in the Status Register will activate the interrupt request (INTRQ). The interrupt line is also activated with normal completion or abnormal termination of all controller operations. The INTRQ signal remains active until reset by reading the Status Register to the processor or by the loading of the Command Register. In addition, the INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The Floppy Disk interface consists of head positioning controls, write gate controls, and data transfers. A 2.0 MHz ± 1% square wave clock is required at the CLK input for internal control timing, (may be 1.0 MHz for mini floppy.)

HEAD POSITIONING

Four commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and O of the command word. After the last directional step an additional 10 milliseconds of head settling time takes place. The four programmable stepping rates are tabulated below.

The rates (shown in Table 1) can be applied to a Three Phase Motor or a Step-Direction Motor through the device interface. When the $\overline{3PM}$ input is connected to ground the device operates with a three-phase motor control interface, with one active low signal per phase on the three output signals $\overline{PH1}$, $\overline{PH2}$ and PH3. The stepping sequence, when stepping in, is Phases 1-2-3-1, and when stepping out, Phases 1-3-2-1. Phase 1 is active low after Master Reset. Note: PH3 needs an inverter if used.

The Step-Direction Motor Control interface is activated by leaving input $\overline{3PM}$ open or connecting it to +5V. The Phase 1 pin $\overline{PH1}$ becomes a Step pulse of 4 microseconds width. The Phase 2 pin $\overline{PH2}$ becomes a direction control with a high voltage on this pin indicating a Step In, and a low voltage indicating a Step Out. The Direction output is valid a minimum of 24 µs prior to the activation of the Step pulse.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 in the command word to a logic 1. The verification operation begins at the end of the 10 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track

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Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete. If track comparison is not made but the CRC checks, an interrupt is generated, the Seek Error status (Bit 4) is set and the Busy status bit is reset.

TABLE 1
STEPPING RATES

r1	r0	1771-X1 CLK=2MHZ TEST=1	1771-X1 CLK=1MHZ TEST=1	1771 or-X1 CLK=2MHZ TEST=0	1771 or-X1 CLK=1MHZ TEST=0
0	0	6ms	12ms	*APPROX. 400us	*APPROX. 800us
0	1	6ms	12ms		
1	0	10ms	20ms		
1	1	20ms	40ms		

*For exact times consult WDC.

The Head Load (HLD) output controls the movement of the read/write head against the disk for data recording or retrieval. It is activated at the beginning of a Read, Write (E Flag On) or Verify Operation, or a Seek or Step operation with the head load bit, h, a logic one remains activated until the third index pulse following the last operation which uses the read/write head. Reading or Writing does not occur until a minimum of 10 msec delay after the HLD signal is made active. If executing the type 2 commands with the E flag off, there is no 10 msec delay and the head is assumed to be engaged. The delay is determined by sampling of the Head Load Timing (HLT) input after 10 msec. A high state input, generated from the Head Load output transition and delayed externally, identifies engagement of the head against the disk. In the Seek and Step commands, the head is loaded at the start of the command execution when the h bit is a logic one. In a verify command the head is loaded after stepping to the destination track on the disk whenever the h bit is a logic zero.

DISK READ OPERATION

The 2.0 MHz external clock provided to the device is internally divided by 4 to form the 500 KHz clock rate for data transfer. When reading data from a diskette this divider is synchronized to transitions of the Read Data (FDDATA) input. When a transition does not occur on the 500 KHz clock active state, the clock divider circuit injects a clock to maintain a continuous 500 KHz data clock. The 500 KHz data clock is further divided by 2 internally to separate the clock and information bits. The divider is phased to the information by the detection of the address mark.

In the internal data read and separation mode the Read Data input toggles from one state to the opposite state for each logic one bit of clock or information. This signal can be derived from the amplified, differentiated, and sliced Read Head signal, or by the output of a flip-flop toggling on the Read Data pulses. This input is sampled by the 2 MHz clock to detect transitions.

The chip can also operate on externally separated data, as supplied by methods such as Phase Lock loop, One Shots, or variable frequency oscillators. This is accomplished by grounding the External Data Separator ($\overline{XTDS}$) INPUT. When the Read Data input makes a high to-low transition, the information input to the FDDATA line is clocked into the Data Shift Register. The assembled 8 bit data from the Data Shift Register are then transferred to the Data Register.

The normal sector length for Read or Write operations with the IBM 3740 format is 128 bytes. This format or binary multiples of 128 bytes will be adopted by setting a logic 1 in Bit 3 of the Read and Write commands. Additionally, a variable sector length feature is provided which allows an indicator recorded in the ID Field to control the length of the sector. Variable sector lengths can be read or written in Read or Write commands respectively by setting a logic o in Bit 3 of the command word. The sector length indicator specifies the number of 16 byte groups or 16 x N, where N is equal to 1 to 256 groups. An indicator of all zeroes is interpreted as 256 sixteen byte groups.

DISK WRITE OPERATION

After data is loaded from the processor into the Data Register, and is transferred to the Data Shift Register, data will be shifted serially through the Write Data (WD) output. Interlaced with each bit of data is a positive clock pulse of 0.5 µsec duration. This signal may be used to externally toggle a flip-flop to control the direction of Write Current flow.

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD1771 before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The $\overline{\text{Write Fault}}$ input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD1771 terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the Write Gate output becomes inactive.

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Whenever a Read or Write command is received the FD1771 samples the READY input. If this input is logic low the command is not executed and an interrupt is generated. The Seek or Step commands are performed regardless of the state of the READY input.

COMMAND DESCRIPTION

The FD1771 will accept and execute eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in table 2.

COMMAND SUMMARY*

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	$\overline{s}$
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

TABLE 2

* = Shown in true form.

FLAG SUMMARY

TYPE 1

h = Head Load Flag (Bit 3)
- h=1, Load head at beginning
- h=0, Do not load head at beginning

V = Verify flag (Bit 2)
- V=1, Verify on last track
- V=0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)
- Refer to Table 1 for rate summary

u = Update flag (Bit 4)
- u=1, Update Track register
- u=0, No update

TABLE 3

TYPE II

m = Multiple Record flag (Bit 4)
- m =0, Single Record
- m =1, Multiple Records

b = Block length flag (Bit 3)
- b =1, IBM format (128 to 1024 bytes)
- b =0, Non-IBM format (16 to 4096 bytes)

a_1a_0 =Data Address Mark (Bits 1-0)
- a_1a_0 =00, FB (Data Mark)
- a_1a_0 =01, FA (User defined)
- a_1a_0 =10, F9 (User defined)
- a_1a_0 =11, F8 (Deleted Data Mark)

TABLE 4

TYPE III

s =Synchronize flag (Bit 0)
- $\overline{s}$=0, Synchronize to AM
- $\overline{s}$=1, Do Not Synchronize to AM

TYPE IV

Ii =Interrupt Condition flags (Bits 3-0)
- I_0=1, Not Ready to Ready Transition
- I_1=1, Ready to Not Ready Transition
- I_2=1, Index Pulse
- I_3=1, Immedate interrupt

E =Enable HLD and 10 msec Delay
- E=1, Enable HLD, HLT and 10 msec Delay
- E=0, Head is assumed Engaged and there is no 10 msec Delay.

TABLE 5

TYPE 1 COMMANDS

The Type 1 Commands include the RESTORE, SEEK STEP, STEP-IN, AND STEP-OUT commands. Each of the Type 1 Commands contain a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 1, page four.

The type 1 Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command(HLD output is made active). If h = 0,HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD1771 receives a command that specifically disengages the head. If the FD1771 does not receive any commands after two revolutions of the disk, the head will be automatically disengaged (HLD made inactive). The Head Load Timing Input is sampled after a 10 ms delay, when reading or writing on the disk is to occur.

The Type 1 Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V = 1, a verification is performed, if V = 0, no verification is performed.

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During verification, the head is loaded and after an internal 10 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the BUSY status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, the Seek Error status bit (Status bit 4) is set and the BUSY status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after two revolutions of the disk, the FD1771 terminates the operation and sends an interrupt, (INTRQ).

The STEP, STEP-IN, and STEP-OUT commands contain an UPDATE flag (U). When U = 1, the track register is updated by one for each step. When U = o, the track register is not updated.

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{TROO}$) input is sampled. If $\overline{TROO}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TROO}$ is not active low, stepping pulses (pins 15 to 17) at a rate specified by the r1r0 field are issued until the $\overline{TROO}$ input is activated. At this time the TR is loaded with zeroes and an interrupt is generated. If the $\overline{TROO}$ input does not go active low after 255 stepping pulses, the FD1771 terminates operation, interrupts, and sets the Seek error status bit. Note that the RESTORE command is executed when $\overline{MR}$ goes from an active to an inactive state. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD1771 will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the data register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD1771 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the u flag is on, the TR is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

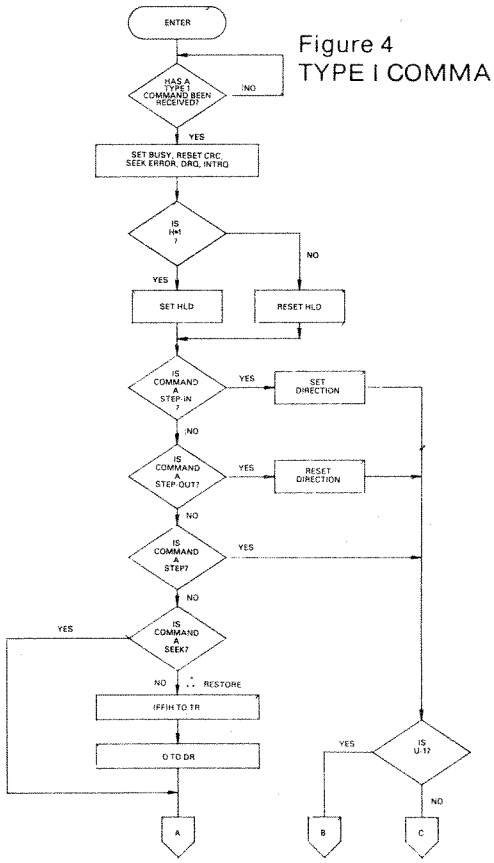

Figure 4
TYPE I COMMAND FLOW

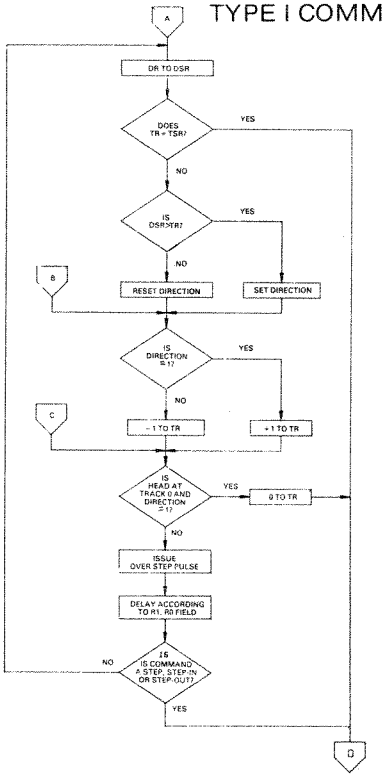

Figure 5
TYPE I COMMAND FLOW

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STEP-IN

Upon receipt of this command, the FD1771 issues one stepping pulse in the direction towards track 76. If the u flag is on the Track Register is incremented by one. After a delay determined by the r_1 r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD1771 issues one stepping pulse in the direction towards track 0. If the u flag is on, the TR is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

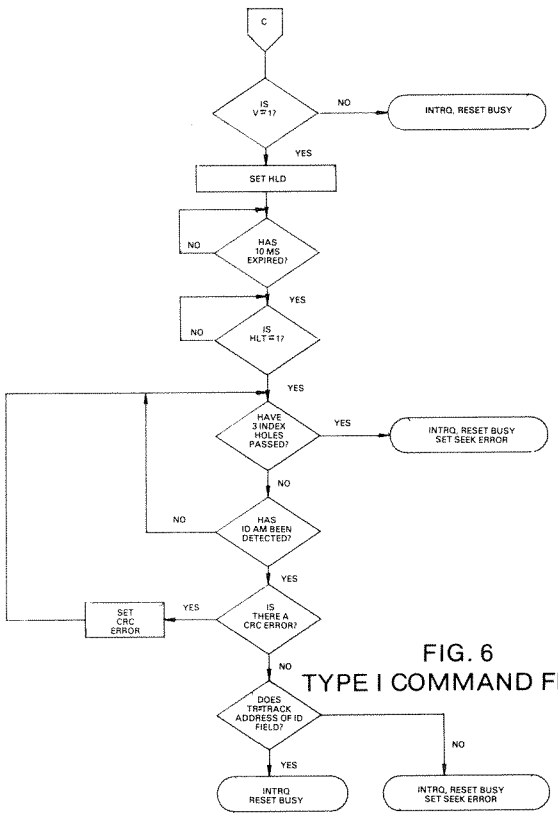

FIG. 6
TYPE I COMMAND FLOW

*NOTE: *1. IF $\overline{TEST}$ = 0, THERE IS NO 10MS DELAY.
2. IF $\overline{TEST}$ = 1 AND CLK = 1 MHz, THIS IS A 20MS DELAY.

TYPE II COMMANDS

The Type II Commands include the Read Sector (s) and Write Sector (s) commands. Prior to loading the type II command into the COMMAND REGISTER, the computer must load the Sector Register with the desired sector number. Upon receipt of the type II command, the busy status Bit is set. If the E flag =1 (this is the normal case) HLD is made active and HLT is sampled after a 10 msec delay. If the E flag is0, the head is assumed to be engaged and there is no 10 msec delay. The ID field and Data Field format are shown below:

When an ID field is located on the disk, the FD1771 compares the Track Number of the ID field with the Track register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD1771 must find an Id field with a Track number, Sector number, and CRC within two revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

GAP	ID AM	TRACK NUMBER	ZEROS	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD									DATA FIELD			

IDAM = ID Address Mark — DATA=$(FE)_{16}$ CLK = $(C7)_{16}$
Data AM = Data Address Mark — DATA=(F8, F9, FA, or FB), CLK = $(C7)_{16}$

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Each of the Type II Commands contain a (b) flag which in conjunction with the sector length field contents of the ID determines the length (number of characters) of the Data field.

For IBM 3740 compatibility, the b flag should equal 1. The numbers of bytes in the data field (sector) is then 128 x 2^n where n - 0,1,2,3.

For b = 1

Sector Length Field (hex)	Number of bytes in sector (decimal)
00	128
01	256
02	512
03	1024

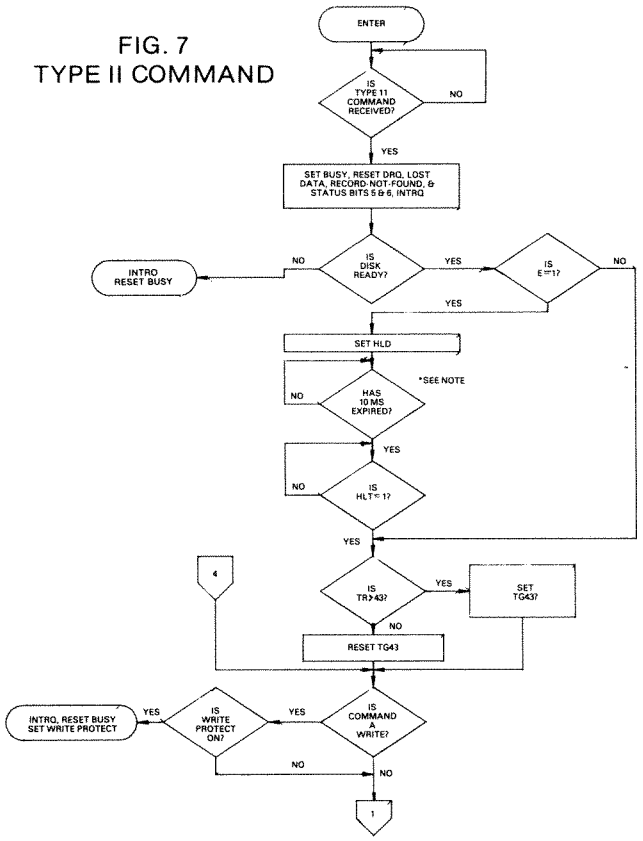
When the b flag equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field as shown below:

For b = 0

Sector Length Field (hex)	Number of bytes in sector (decimal)
01	16
02	32
03	48
04	64
•	•
•	•
•	•
FF	4080
00	4096

Each of the type II commands also contain a (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = o a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1 , multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD1771 will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the command register, which terminated the command and generates an interrupt.

FIG. 7
TYPE II COMMAND



*1. IF TEST = 0, THERE IS NO 10MS DELAY.
2. IF TEST = 1 AND CLK = 1 MHz, THIS IS A 20MS DELAY.

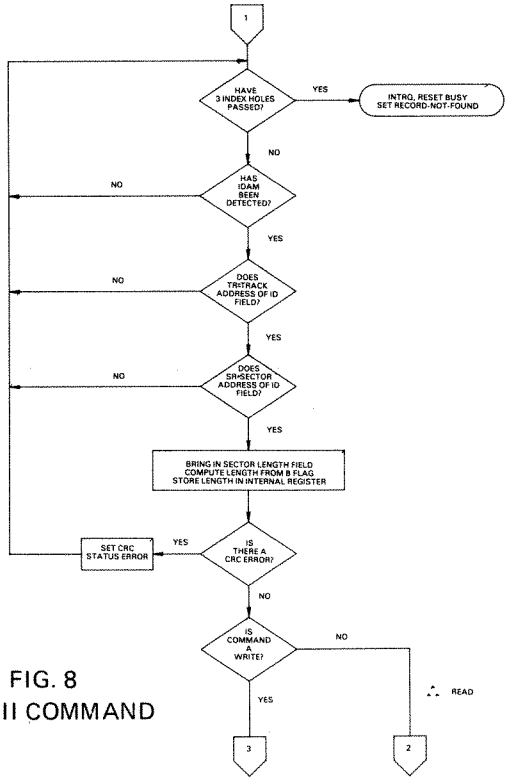


FIG. 8
TYPE II COMMAND

READ COMMAND

Upon receipt of the Read command, the head is loaded, the BUSY status bit set, and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 28 bytes of the correct field; if not, the Record Not Found status bit is set and the operation is terminated. When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bits 5 and 6) as shown below:

Status Bit 5	Status Bit 6	Data AM (HEX)
0	0	FB
0	1	FA
1	0	F9
1	1	F8

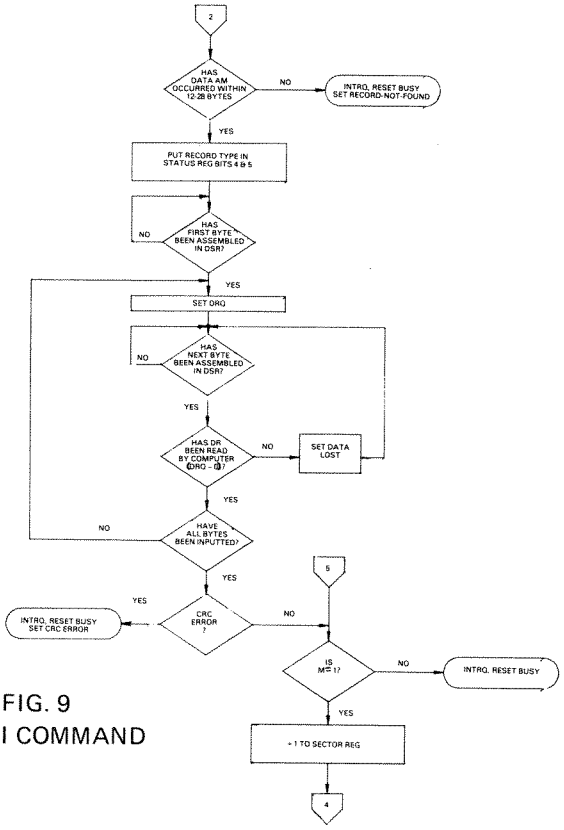


FIG. 9
TYPE II COMMAND

WRITE COMMAND

Upon receipt of the Write command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The FD1771 counts off 11 bytes from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a^1a^0 field of the command as shown below:

a1	a0	DATA MARK (HEX)	CLOCK MARK (HEX)
0	0	FB	C7
0	1	FA	C7
1	0	F9	C7
1	1	F8	C7

The FD1771 then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte gap of logic ones. The WG output is then deactivated.

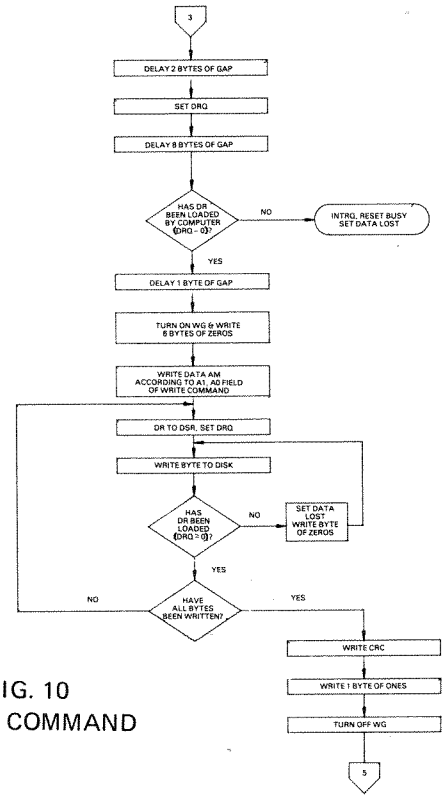


FIG. 10
TYPE II COMMAND

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the BUSY Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	ZEROS	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FD1771 checks for validity and the CRC error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the BUSY Status is reset.

READ TRACK

Upon receipt of the Read Track command, the head is loaded and the BUSY Status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If bit O (S) of the command is a 0, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

WRITE TRACK

Upon receipt of the Write Track command, the head is loaded and the BUSY Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon recieving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR When needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR.

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN (HEX)	INTERPRETATION	CLOCK MARK (HEX)
F7	Write CRC Char.	FF
F8	Data Addr. Mark	C7
F9	Data Addr. Mark	C7
FA	Data Addr. Mark	C7
FB	Data Addr. Mark	C7
FC	Index Addr. Mark	D7
FD	Spare	
FE	ID Addr. Mark	C7

The Write Track command will not execute if the $\overline{DINT}$ input is grounded; instead the Write Protect Status bit is set and the interrupt is activated. Note that one F7 pattern generates 2 CRC characters.

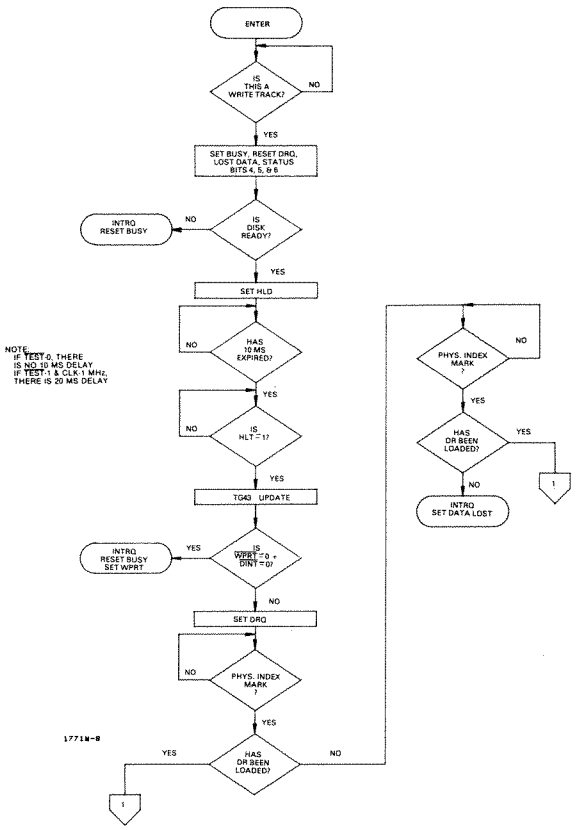


FIG. 11
TYPE III COMMAND
WRITE TRACK

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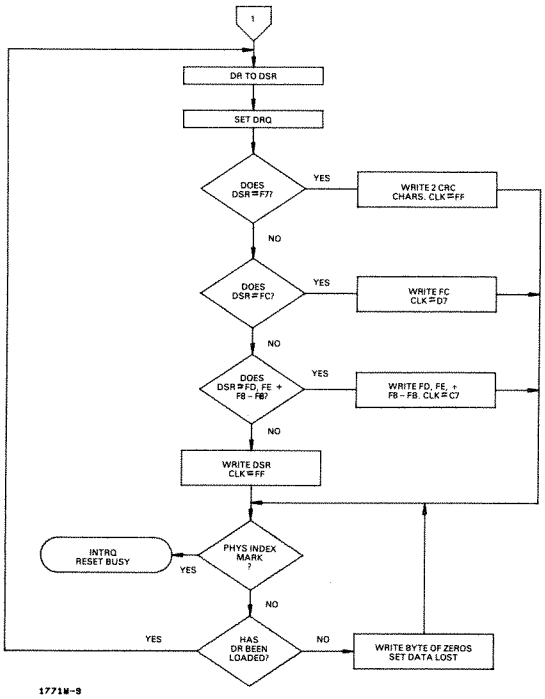

FIG. 12
TYPE III COMMAND
WRITE TRACK

TYPE IV COMMAND

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0 = Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

NOTE: If I_0I_3=0,, there is no interrupt generated but the current command is terminated and busy is reset.

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the BUSY Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the BUSY status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, theBUSY Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below:

(BITS)

7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD ENGAGED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

TABLE 6

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STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the READY input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	When set, there was one or more CRC errors encountered on an unsuccessful track verification operation. This bit is reset to 0 when updated.
S2 Track 00	When set, indicates Read Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TROO}}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS BITS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the READY input and 'ored' with MR. The TYPE II and III Commands will not execute unless the drive is ready.
S6 RECORD TYPE/ WRITE PROTECT	On read Record: In indicates the MSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the LSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND	When set, it indicates that the desired track and sector were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

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FORMATTING THE DISK
(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/0 or when operating under DMA control with a large amount of memory. When operating under DMA with limited amount of memory, formatting is a more difficult task. This is because gaps as well as data must be provided at the computer interface.

Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the FD 1771 raises the data request signal. At this point in time, the user loads the data register with desired data to be written on the disk. For every byte of information to be written on the disk, a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a clock mark of $(FF)_{16}$. However, if the FD1771 detects a data pattern on F7 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters. As a consequence, the patterns F7 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by a F7 pattern.

Disks may be formatted in IBM 3740 formats with sector lengths of 128, 256, 512, or 1024 bytes, or may be formatted in non-IBM 3740 with sectors length of 16 to 4096 bytes in 16 byte increments. IBM 3740 at the present time only defines two formats. One format with 128 bytes/sector and the other with 256 bytes/sector. The next section deals with the IBM 3740 format with 128 bytes/sector and the following section details non-IBM formats.

IBM 3740 FORMATS - 128 BYTES/SECTOR

Shown in Figure 13, is the IBM format with 128 bytes/sector. In order to format this format, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

	NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
	40	00 or FF
	6	00
	1	FC (Index Mark)
	26	00 or FF
*	6	00
*	1	FE (ID Address Mark)
*	1	Track Number (0 thru 4C)
*	1	00
*	1	Sector Number (1 thru 1A)
*	1	00
*	1	F7 (2 CRC's written)
*	11	00 or FF
*	6	00
*	1	FB (Data Address Mark)
*	128	Data (IBM uses E5)
*	1	F7 (2 CRC's written)
*	27	00 or FF
	247**	00 or FF

* Write bracketed field 26 times
** Continue writing until FD1771 interrupts out. Approx. 247 bytes.

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NON-IBM FORMATS

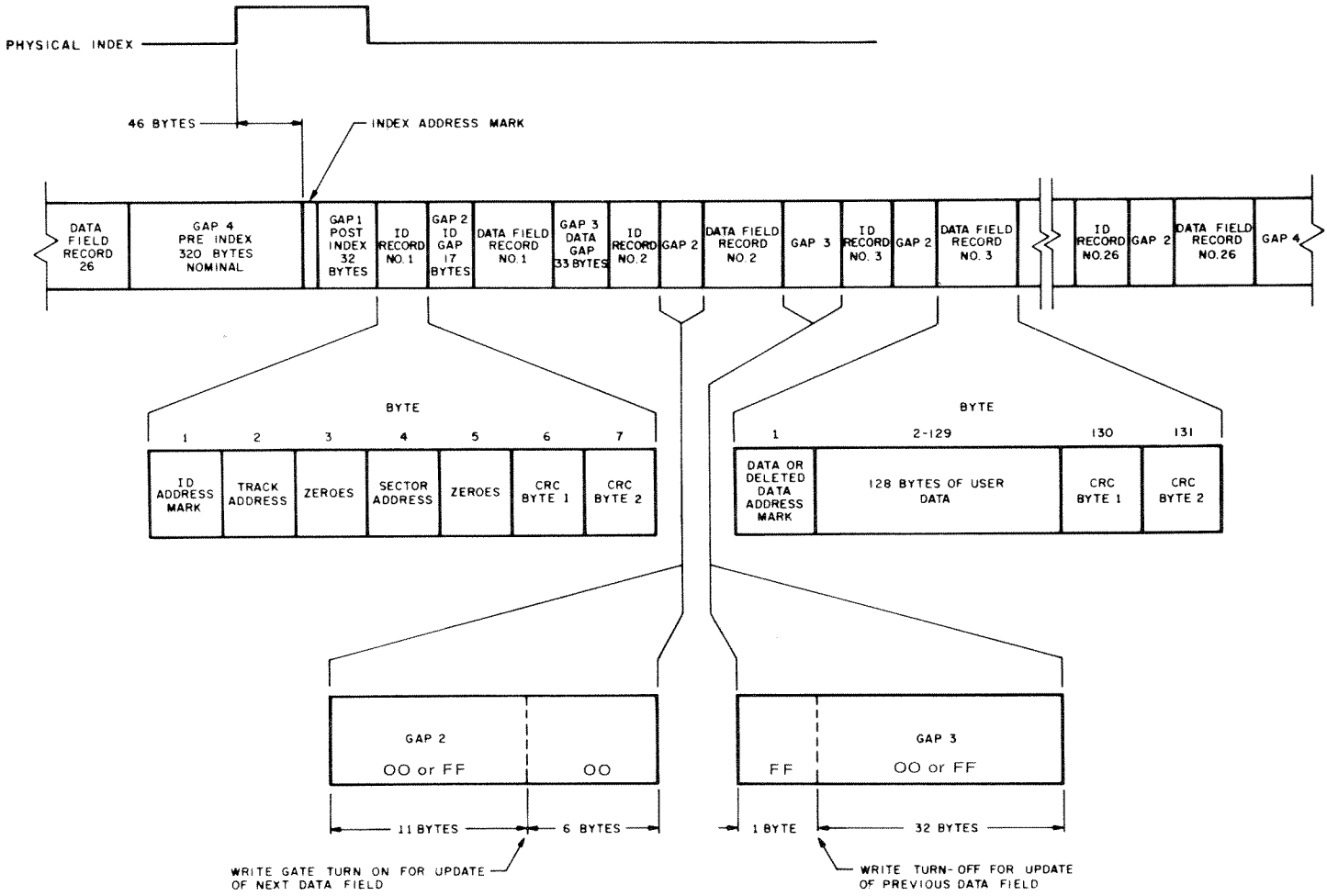
Non IBM Formats are very similar to the IBM formats except a different algorithum is used to ascertain the sector length from the sector length byte in the ID field. This permits a wide range of sector lengths from 16 to 4096 bytes. Refer to section V, Type II commands with b flag equal to zero. Note that F7 thru FE must not appear in the sector length byte of the ID field.

In formatting the FD1771, only two requirements regarding GAP sizes must be met. GAP 2 (i.e., the gap between the ID field and data field)must be 17 bytes of which the last 6 bytes must be zero and that every address mark be preceded by at least one byte of zeros. However, it is recommended that every GAP be at least 17 bytes long with 6 bytes of zeros. The FD1771 does not require the index address mark (i.e., DATA = FC, CLK = D7) and need not be present.

References:

1) IBM Diskette OEM Information GA21-9190-1
2) SA900 IBM Compatibility Reference Manual - Shugart Associates.

FIG.13
TRACK FORMAT



ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{DD} With Respect to V_{BB} (Ground)	+20 to −0.3V
Max Voltage to Any Input With Respect to V_{BB}	+20 to −0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	−55°C to +125°C

OPERATING CHARACTERISTICS (DC)

T_A = ØºC to 7ØºC, V_{DD} = +12.ØV ± .6V, V_{BB}*= –5.Ø ± .5V, V_{SS}= ØV, V_{CC} = +5V ± .25V
V_{DD} = 10 ma Nominal, V_{CC} = 30 ma Nominal, V_{BB}*= 0.4 µa Nominal

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leagage			10	µA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	µA	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6			V	
V_{IL}	Input Low Voltage (All Inputs)			0.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = –100 uA
V_{OL}	Output Low Voltage			0.45**	V	I_O = 1.6 mA

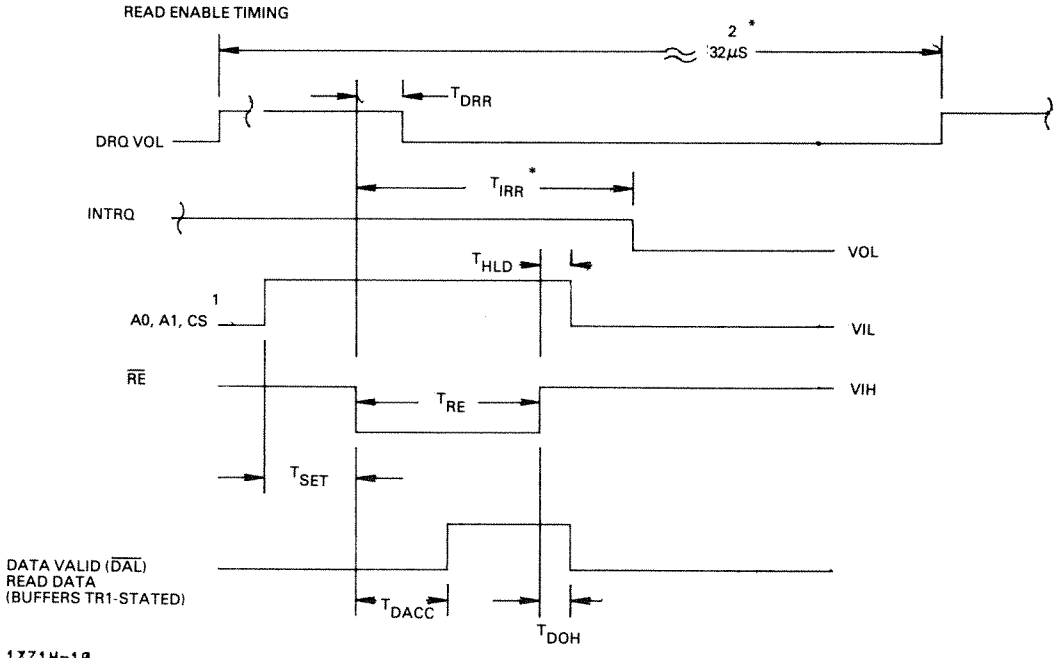
NOTE: Vol ≤ .4V when interfacing with low Power Schottky parts (I_O<1 ma) **Write Gate V_{OL}≤0.5V

TIMING CHARACTERISTICS

T_A = ØºC to 70ºC, V_{DD} = +12V ± .6V, V_{BB}*= –5 ± .25V, V_{SS} = ØV, V_{CC} = +5 ± .25V
NOTE: Timings are given for 2 MHZ Clock. For those timings noted, values will double when chip is operated at 1 MHZ. Use 1 MHZ when using mini-floppy.
*V_{BB} required for –01 version only. Pin 1 (V_{BB}) is left open on –11 version.

Read Operations

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	500			nsec	C_L = 25 pf
TDRR	DRQ Reset from $\overline{RE}$			500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$			3000	nsec	
TDACC	Data Access from $\overline{RE}$			450	nsec	C_L= 25 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C_L = 25 pf



NOTE: 1. $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED.
2. FOR READ TRACK COMMAND, THIS TIME MAY BE 12* TO 32*µSEC WHEN S = 0.
*TIME DOUBLES WHEN CLK – 1MHz.

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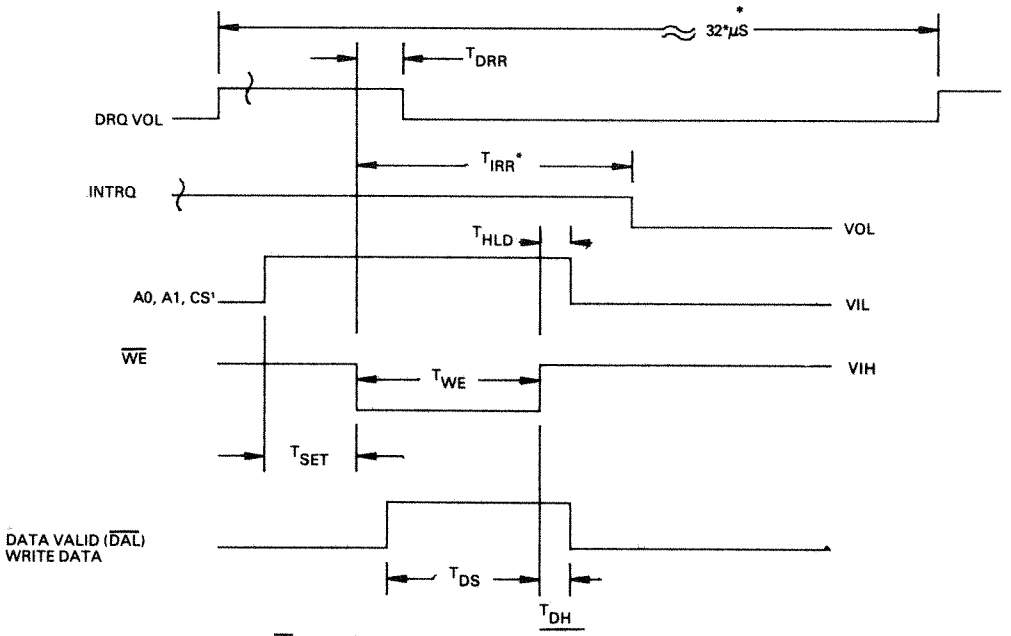
Write Operations

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$			500	nsec	See Note
TIRR	INTRQ Reset from $\overline{WE}$			3000	nsec	
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	150			nsec	

WRITE ENABLE TIMING



NOTE: 1. $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED.
2. WHEN WRITING DATA INTO SECTOR, TRACK, OR DATA REGISTER, USER CANNOT READ THIS REGISTER UNTIL AT LEAST 8µSEC AFTER THE RISING EDGE OF $\overline{WE}$. WHEN WRITING INTO THE COMMAND REGISTER, STATUS IS NOT VALID UNTIL SOME 12µSEC LATER. THESE TIMES ARE DOUBLED WHEN CLK = 1MHz.

* = TIME DOUBLES WHEN CLK = 1 MHz.

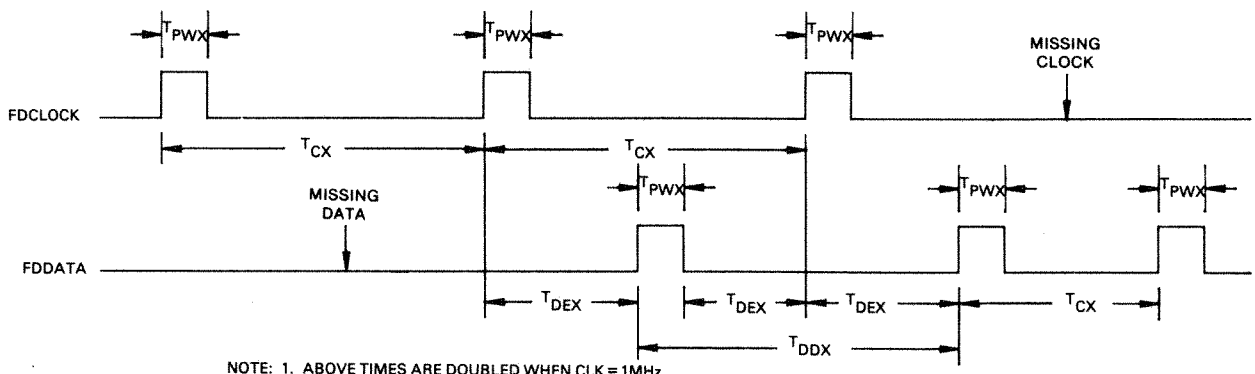
External Data Separation ($\overline{XTDS}$ = 0)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TPWX	Pulse Width Rd Data & Rd Clock	150		350	nsec	
TCX	Clock Cycle Ext	2500			nsec	
TDEX	Data to Clock	500			nsec	
TDDX	Data to Data Cycle	2500			nsec	

READ TIMING

$\overline{XTDS}$ = 0
EXTERNAL DATA SEPARATION

NOTE: FDCLK & FDDATA may be reversed FD1771 decides what is clock and what is data



NOTE: 1. ABOVE TIMES ARE DOUBLED WHEN CLK = 1MHz.
2. CONTACT WDC FOR EXTERNAL CLOCK/DATA SEPARATOR CIRCUITS.

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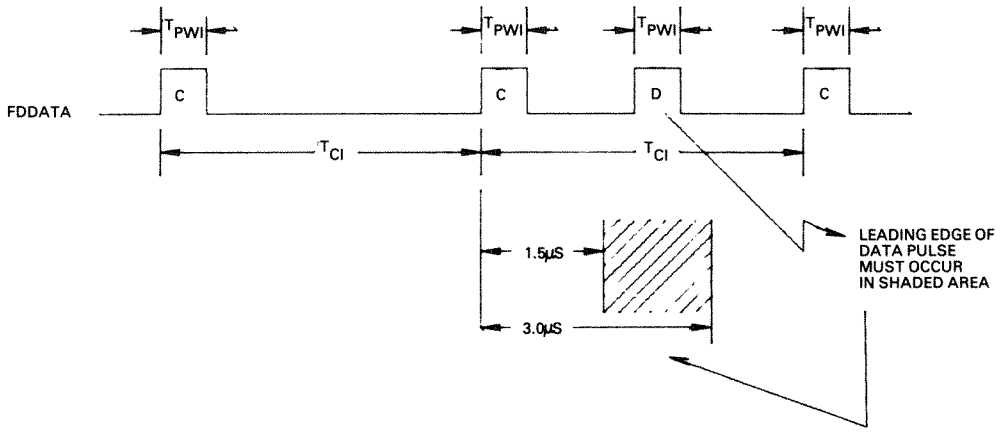
Internal Data Separation ($\overline{XTDS}$ = 1)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TPWI	Pulse Width Data & Clock	150		1000	nsec	
TCI	Clock Cycle Internal	3500		5000	nsec	

READ TIMING

$\overline{XTDS}$ = 1
INTERNAL DATA SEPARATION
FDCLOCK MUST BE TIED HIGH

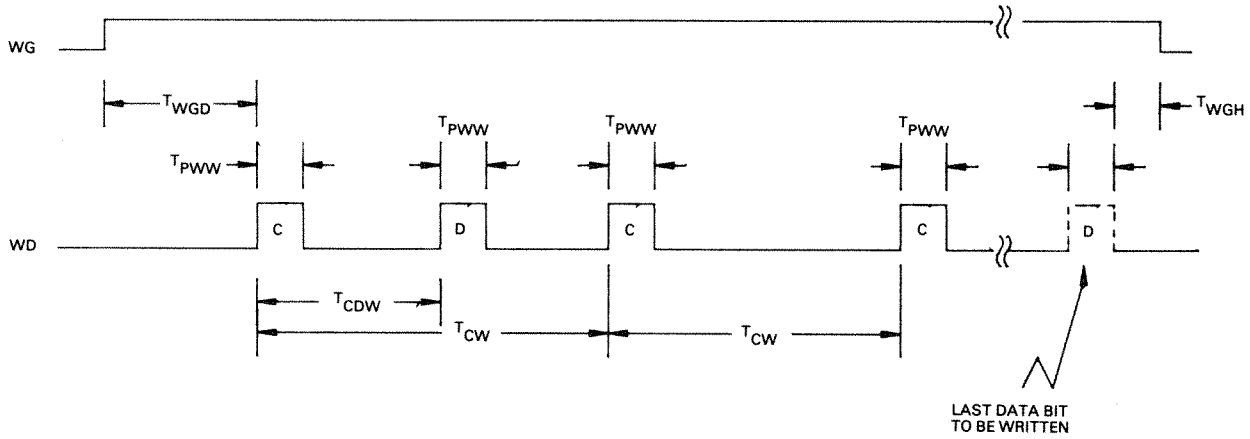


NOTE: INTERNAL DATA SEPARATION MAY WORK FOR SOME APPLICATIONS. HOWEVER, FOR APPLICATIONS REQUIRING HIGH DATE RECOVERY RELIABILITY, WDC RECOMMENDS EXTERNAL DATA SEPARATION BE USED.

Write Data Timing:

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TWGD	Write Gate to Data		1200		nsec	300 nsec ± CLK tolerance
TPWW	Pulse Width Write Data	500		600	nsec	
TCDW	Clock to Data		2000		nsec	±0.5%± CLK tolerance
TCW	Clock Cycle Write		4000		nsec	±0.5%± CLK tolerance
TWGH	Write Gate Hold to Data	0		100	nsec	

WRITE DATA TIMING



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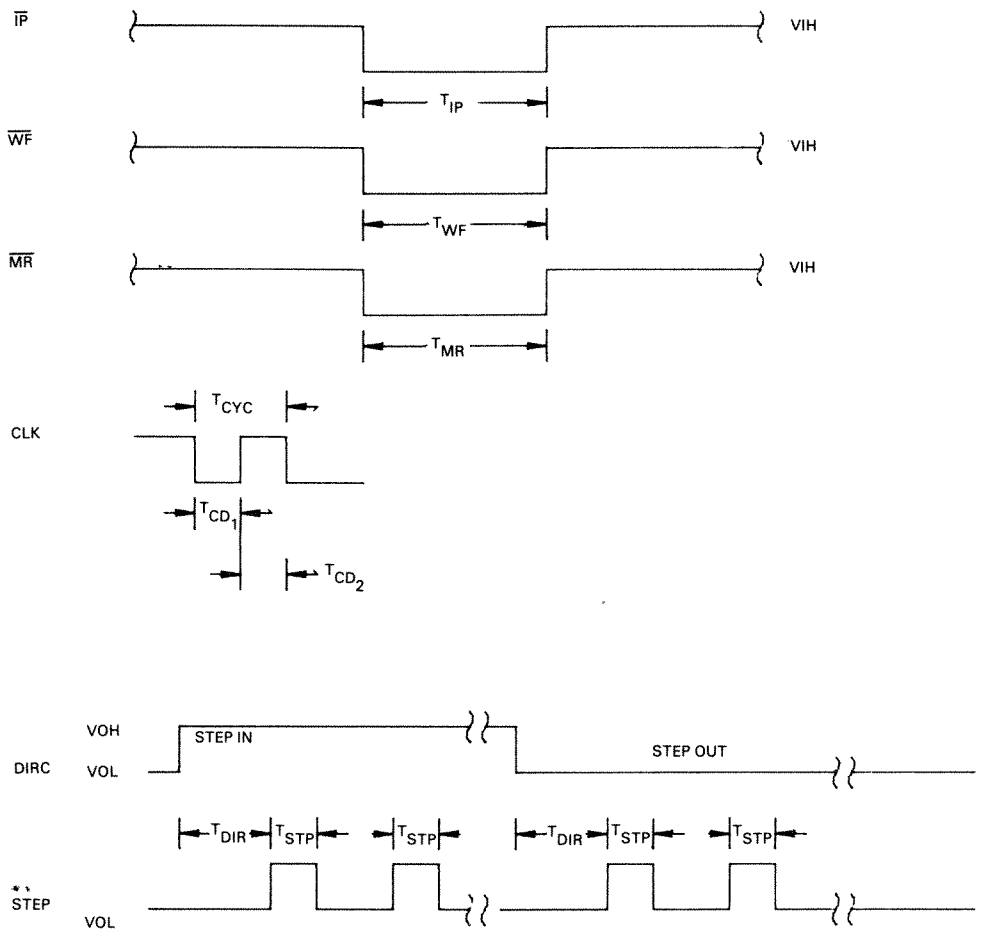
Miscellaneous Timing:

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TCD_1	Clock Duty	175			nsec	2MHZ ±1% See Note
TCD_2	Clock Duty	210			nsec	
TSTP	Step Pulse Output	3800		4200	nsec	
TDIR	Dir Setup to Step	24			µsec	These times doubled when CLK = 1 MHZ
TMR	Master Reset Pulse Width	10			µsec	
TIP	Index Pulse Width	10			µsec	
TWF	Write Fault Pulse Width	10			µsec	

MISCELLANEOUS TIMING



PIN OUTS

PIN NO.	PIN NAME	SYMBOL	FUNCTION
1	Power Supplies	V_{BB}/NC	−5V for −01 version/open for −11 version
20		V_{SS}	Ground
21		V_{CC}	+5V
40		V_{DD}	+12V
19	MASTER RESET	MR	• A logic low on this input resets the device and loads "03" into the command register. The Not Ready (Status Bit 7) is reset during MR ACTIVE. When MR is brought to a logic high a Restore Command is executed, regardless of the state of the Ready signal from the drive.

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PIN NO	PIN NAME	SYMBOL	FUNCTION
Computer Interface:			
7-14	DATA ACCESS LINES	$\overline{DAL}$Ø-$\overline{DAL}$7	• Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by $\overline{WE}$ or a transmitter enabled by $\overline{RE}$.
3	CHIP SELECT	$\overline{CS}$	• A logic low on this input selects the chip and enables computer communication with the device.
5,6	REGISTER SELECT LINES	A0, A1	•These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: A1 A0 $\overline{RE}$ $\overline{WE}$ 0 0 Status Reg Command Reg 0 1 Track Reg Track Reg 1 0 Sector Reg Sector Reg 1 1 Data Reg Data Reg
4	READ ENABLE	$\overline{RE}$	•A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
2	WRITE ENABLE	$\overline{WE}$	•A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
38	DATA REQUEST	DRQ	•This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operation, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	•This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register. Use 10K pull-up resistor to +5.
24	CLOCK	CLK	•This input requires a free-running 2 MHz ± 1% square wave clock for internal timing reference.
Floppy Disk Interface:			
25	EXTERNAL DATA SEPARATION	$\overline{XTDS}$	•A logic low on this input selects external data separation. A logic high or open selects the internal data separator.
26	FLOPPY DISK CLOCK (External Separation)	FDCLOCK	•This input receives the externally separated clock when $\overline{XTDS}$ = 0. If $\overline{XTDS}$ = 1, this input should be tied to a logic high.
27	FLOPPY DISK DATA	FDDATA	•This input receives the raw read disk data if $\overline{XTDS}$ = 1, or the externally separated data if $\overline{XTDS}$ = 0.
31	WRITE DATA	WD	•This output contains both clock and data bits of 500 ns duration.
28	HEAD LOAD	HLD	•The HLD output controls the loading of the Read-Write head against the media. The HLT input is sampled after 10 ms. When a logic high is sampled on the HLT input the head is assumed to be engaged.
23	HEAD LOAD TIMING	HLT	
15	$\overline{Phase\ 1}$/Step	$\overline{PH1}$/STEP	•If the $\overline{3PM}$ input is a logic low the three phase motor control is selected and $\overline{PH1}$, $\overline{PH2}$, and PH3 outputs form a one active low signal out of three. $\overline{PH1}$ is active low after $\overline{MR}$. If the $\overline{3PM}$ input is a logic high the step and direction motor control is selected. The step output contains a 4µsec high signal for each step and the direction output is active high when stepping in; active low when stepping out.
16	$\overline{Phase\ 2}$/Direction	$\overline{PH2}$/DIRC	
17	Phase 3	PH3	
18	$\overline{3\ Phase\ Motor\ Select}$	$\overline{3PM}$	

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PIN NO.;	PIN NAME;	SYMBOL;	FUNCTION
29	Track Greater Than 43	TG43	•This output informs the drive that the Read-Write head is positioned between track 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	•This output is made valid when writing is to be performed on the diskette.
32	Ready	READY	•This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. A Seek operation is performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$	$\overline{\text{WF}}$	•This input detects writing faults indications from the drive. When WG = 1 and $\overline{\text{WF}}$ goes low the current Write command is terminated and the Write Fault status bit is set. The $\overline{\text{WF}}$ input should be made inactive (high) when WG becomes inactive.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	•This input informs the FD1771 that the Read-Write head is positioned over Track 00 when a logic low.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	•Input, when low for a minimum of 10 µsec, informs the FD1771 when an index mark is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	•This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	$\overline{\text{DISK INTIALIZATION}}$	$\overline{\text{DINT}}$	•The input is sampled whenever a Write Track command is received. If $\overline{\text{DINT}}$ = 0, the operation is terminated and the Write Protect Status bit is set.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	•This input is used for testing purposes only and should be tied to +5V or left open by the user.

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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